

Project Name: San Bernardino
PCB Number: 16561-1
PCBA Version: A00
SCH Version: A00
Project Code: 3PD06U010001,3PD06U01A001
PCB certification number: SB0601
ECO# number: 938383
PCB Size: 178.5mm x 174mm x 1.6mm, 6L

JMP1 Jumper Setting		
Service Mode	1-2 Short	With Jumper to Disable TXE
PW CLR	3-4 Open	Without Jumper to Clear PassWord
CMOS CLR	5-6 Short	With Jumper to Clear CMOS
JMP2 Jumper Setting		
Pin9 to 5V	1-3 Short	With Jumper to 5V
Pin1 to 5V	2-4 Short	With Jumper to 5V
Pin9 to RI	3-5 Short	With Jumper to RI
Pin1 to DCD	4-6 Short	With Jumper to DCD

BOM Configuration	
(R_)	Unmount
(X_)	Debug
(64G_)	eMMC 64GB
(16G_)	eMMC 16GB
(32G_)	eMMC 32GB
(T_)	TPM
(2DP_)	DP x2
(3DP_)	DP x3
(AIC_)	Gfx Add-In Card
(RJ45_)	RJ45
(SFP_)	SFP
(GCE_)	GCE PCB vendor
(TRI_)	Tripod PCB vendor
(HSB_)	HSB PCB vendor
(TPT_)	TPT PCB vendor
(A_)	USB-C w/o BC1.2
(B_)	USB-C w/ BC1.2
(E16G_)	5070E w/ 16G
(E_)	5070E
(S16G_)	5070S w/ 16G
(S_)	5070S
(EX16G_)	5070S-EX w/ 16G
(EX_)	5070S-EX
(E32G_)	5070E w/ 32G
(D_)	X02.1

PAGE	TITLE
01	Cover Page
02	Block Diagram
03	(R)
04	(R)
05	CPU (DDR4)
06	CPU (VCCGI/VNN/Others)
07	CPU (VDDQ/VCCRAM/Others)
08	CPU (EDP/DDI/MDSI)
09	(R)
10	CPU (Power CAP1)
11	CPU (Power CAP2)
12	DDR4_SODIMM1
13	DDR4_SODIMM2
14	(R)
15	CPU (STRAP)
16	CPU (PCIE/SATA/USB3/USB2)
17	CPU (I2C/SMB/SPI/UART/CNVI)
18	CPU (PMU/SVID/RTC/ICLK/MSC)
19	CPU (HDA/EMMC/SD/LPC/FSPI)
20	(R)
21	CPU (GPIO/JTAG/ITP)
22	(R)
23	CPU (VSS)
24	ECIO IT8739E/FX
25	Flash ROM/RTC
26	FAN CIRCUITS/HOLE
27	AUDIO CODEC (ALC3253-VA3)
28	HPOUT/GHS1 (FRONT)
29	SPEAKER/GHS2 (REAR)
30	(R)
31	LAN RTL8111HN
32	RJ45_CONN
33	(R)
34	Front USB3.0/USB2.0 Header
35	Rear USB3.0 Stack
36	Front USB2.0 w/ USB Charger
37	Front TYPE-C
38	(R)
39	TYPE-C CC/PD (CCG4)
40	3D3V S0/5V S0
41	3D3V S5/5V S5
42	DCIN JACK
43	(R)
44	V 3P3 A/V 5P0 A (RT6575D)
45	CPU VCORE (RT5092)
46	CPU VCORE VCGI
47	CPU VCORE VNN
48	VDDQ (RT5092_RT9610B)
49	(R)
50	(R)
51	(R)
52	(R)
53	1D8V_S0 (LR9102G)
54	1D2V_S0 (APL5930)
55	eDP to DP+ (PS181)

PAGE	TITLE
56	VGA_CONN
57	DP1_CONN
58	DP2_CONN with PS8468
59	DP3_CONN with PS8468
60	(R)
61	NGFF WLAN (DISCRETE/CNVI)
62	NGFF SSD (SATA)
63	eMMC
64	LED/POWER BUTTON
65	PCIE X4 SLOT
66	LPT1 & COM2_CONN
67	(R)
68	DEBUG CONNECTOR
69	(R)
70	(R)
71	(R)
72	(R)
73	(R)
74	(R)
75	(R)
76	(R)
77	(R)
78	(R)
79	(R)
80	(R)
81	(R)
82	(R)
83	(R)
84	(R)
85	(R)
86	(R)
87	(R)
88	(R)
89	Stitching Capacitors
90	(R)
91	TPM (NPCT750)
92	COM1
93	(R)
94	CAC_CONN
95	USB3.0 HUB1 (RTS5411)
96	USB3.0 HUB2 (RTS5415)
97	SFP RTL8211FS
98	(R)
99	CPU MIPI-60 & APS
100	(R)
101	Cable_List
102	Power Sequence
103	Power Block Diagram
104	Power Good & Reset Diagram
105	Clock Diagram

Key IC		
Location	Vendor part number	IC version
CPU1	Intel Gemini Lake SoC	B0
U2401	ITE IT8739E	FX
U2701	Realtek ALC3253-VA3	A
U3101	Realtek RTL8111HN	A
U3701	Parade PS8743B	B1
U3901	Cypress CYPD4125	A
U5501	Parade PS181	A1
U5801	Parade PS8468	A3
U5901	Parade PS8468	A3
U9101	Nuvoton NPCT750	A
U9501	Realtek RTS5411	A
U9601	Realtek RTS5415	A
U9701	Realtek RTL8211FS	A
U304	Broadcom BCM58102PB0KFBG	P

Header	
FANC1	021.60137.0104
JMP1	021.60810.0203
JMP2	021.60809.0203
PWRSW1	021.60747.0203
USB2F2	021.60892.0210
CAC1	20.F2220.005
SPK1	020.F1062.0006
LPT1	20.F1954.020
COM2	20.F2110.012
RTC1	062.70001.0021
VGA1	020.F0827.0030
LPC1	20.F1819.010
XDP1	20.F1412.040

SVID/SSID	
San Bernardino	
SVID: 0x1028	
SSID: 0x080C	

The PU and PD information for the following straps are different for Pre-ES, ES and ES2, QS GLK SoC.

This is update to information shared in WW28 MoW.

GPIO_83	SIO_SPI_0_TXD	LPC 1.8 V/3.3 V mode select	20K PU [Pre-ES and ES] 20K PD [ES2 ^[1] and QS]	1=buffers set to 1.8 V mode 0=buffers set to 3.3 V mode (default)
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8 V/3.3 V mode select	20K PU [Pre-ES and ES] 20K PD [ES2 ^[1] and QS]	1=buffers set to 1.8 V mode 0=buffers set to 3.3 V mode (default)
GPIO_168	AVS_HDA_SDI	PMU 1.8 V/3.3 V mode select	20K PU [Pre-ES and ES] 20K PD [ES2 ^[1] and QS]	1=buffers set to 1.8 V mode 0=buffers set to 3.3 V mode (default)

^[1]ES2 samples will be limited samples for targeted customers.

SKU ID Settings

SKU6	SKU5	SKU4	SKU3	SKU2	SKU1	Description
U49	U51	U46	U48	AA39	AA41	
Reserve	Reserve	0	0	0	0	Reserve
Reserve	Reserve	0	0	0	1	5070E(W/ eMMC 16GB)
Reserve	Reserve	0	0	1	0	5070E(W/O eMMC 16GB)
Reserve	Reserve	0	0	1	1	5070S(W/ eMMC 16GB)
Reserve	Reserve	0	1	0	0	5070S(W/O eMMC 16GB)
Reserve	Reserve	0	1	0	1	5070S-EX(W/ eMMC 16GB)
Reserve	Reserve	0	1	1	0	5070S-EX(W/O eMMC 16GB)
Reserve	Reserve	0	1	1	1	5070E (W/ eMMC 32GB)

Board ID Settings

MB Version	Board2	Board1
X00 (EVT)	0V	0V
X01 (DVT1)	0V	0.9V
X02 (DVT2)	0V	1.8V
Reserve	0.9V	1.8V
A00 (PVT)	1.8V	1.8V

	5070E (Economy)	5070S (Standard)	5070S Extended
Slim	✓	✓	
Wide			✓

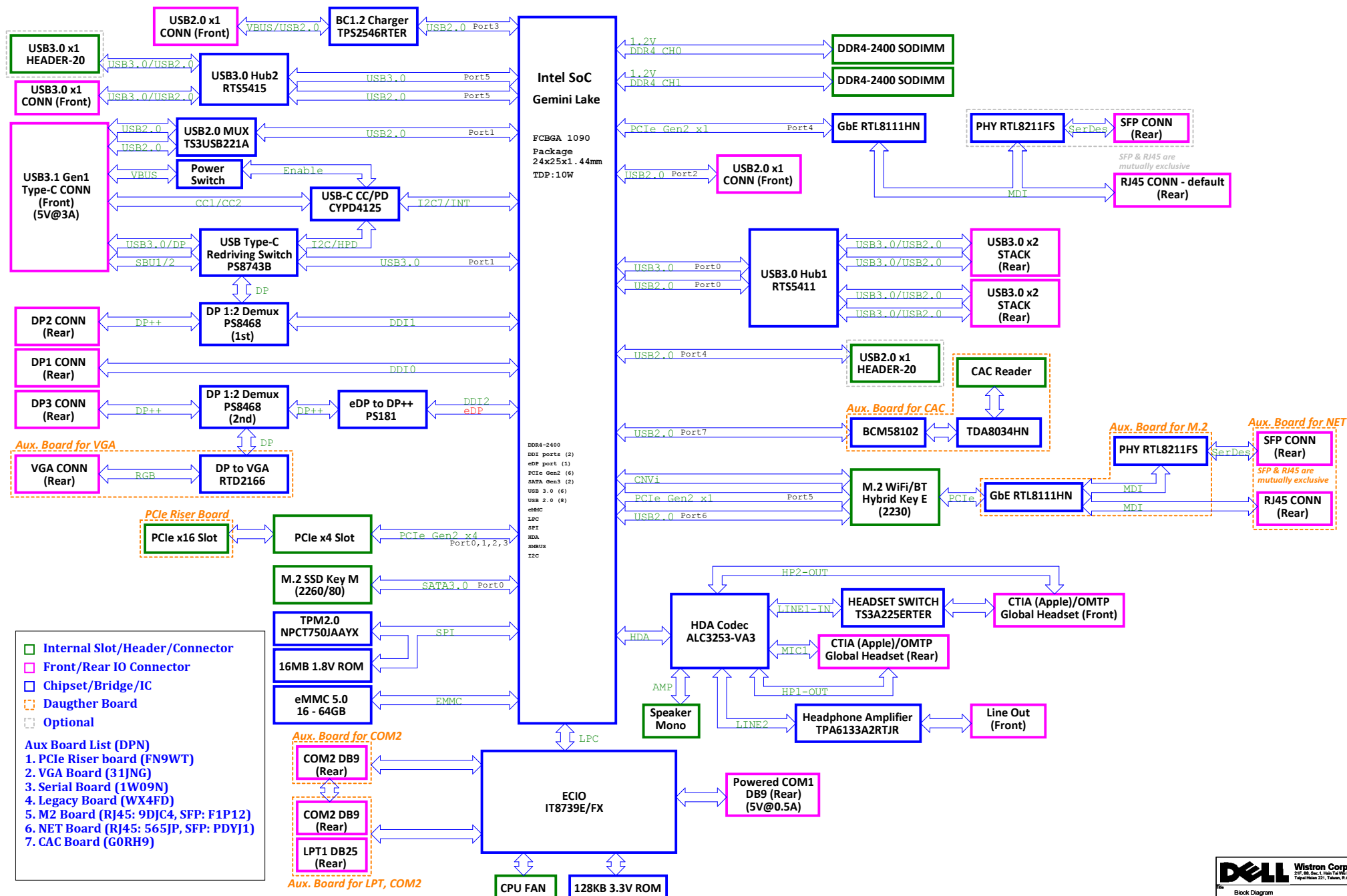
Cable

More detail on Page 101

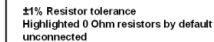
PWB DELL P/N
GCE: WWVX3\$JA
Tripod: WWVX3\$KA
HSB: WWVX3\$CA
TPT: WWVX3\$LA

SoC DELL P/N
Pentium J5005: NJR5K
Celeron J4105: MR9JG

		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size C	Document Number San Bernardino		Rev A00
Date:	Thursday, March 08, 2018	Sheet 1 of	106



Blanking



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

1V_CPU_VCGI ○→ 1V_CPU_VCGI [10.46,64]
1V_CPU_VNN ○→ 1V_CPU_VNN [10.47,89]

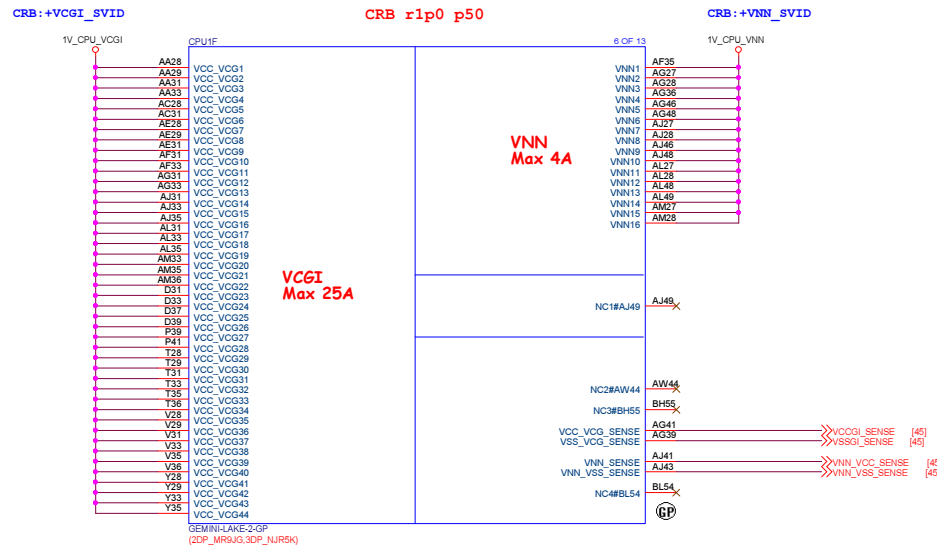
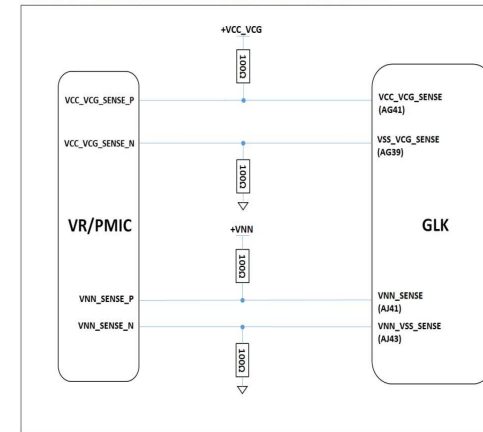
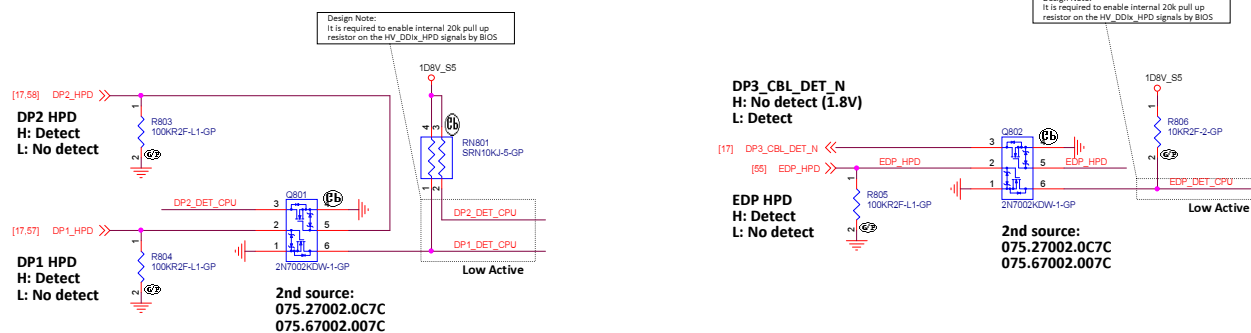
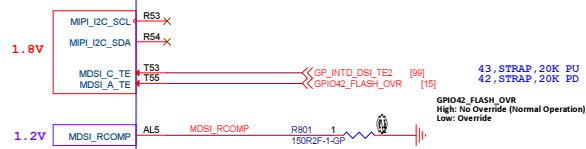
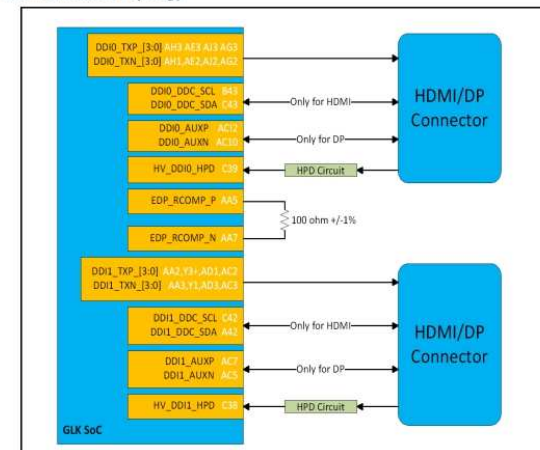
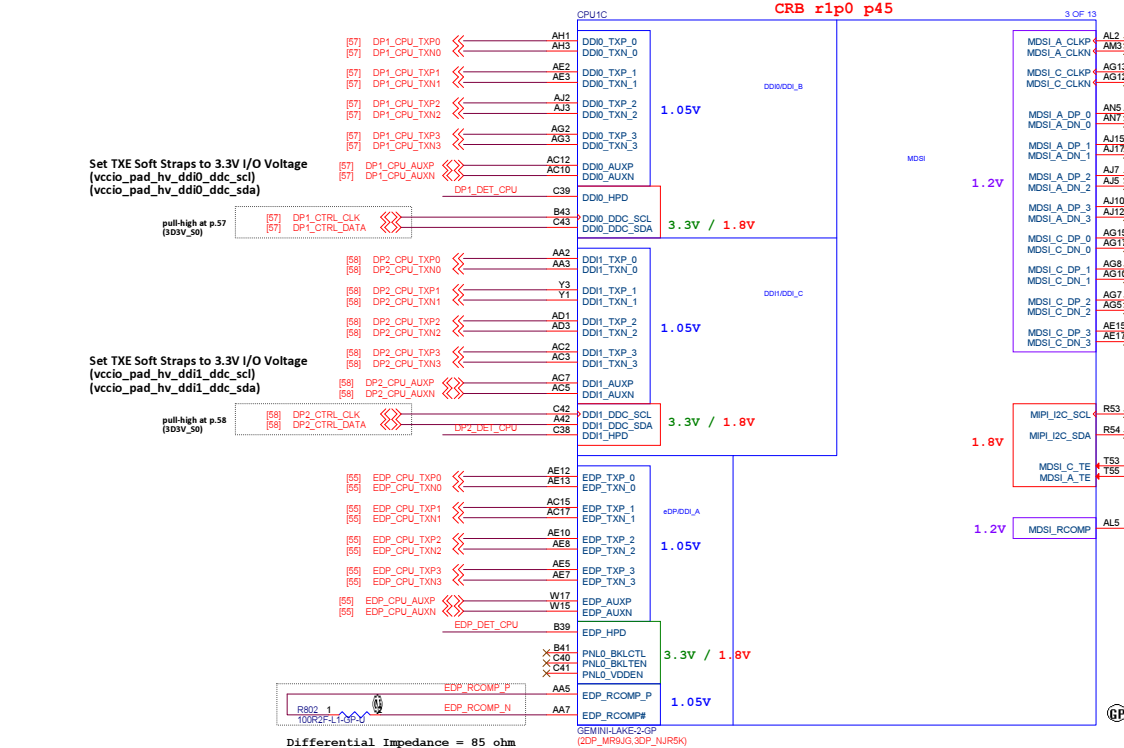


Figure 3-7. VCC_VCG, VSS_VCG and VNN, VNN_VSS Sense Guideline





Blanking

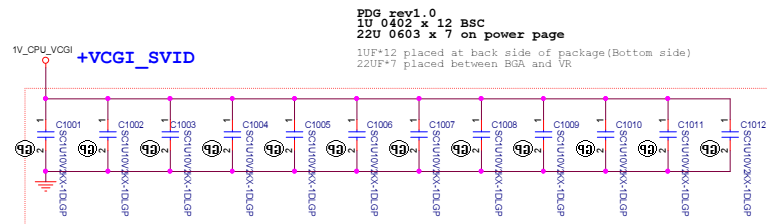
1V_CPU_VCGI 0--> 1V_CPU_VCGI [6.46,64]
1V_CPU_VNN 0--> 1V_CPU_VNN [6.47,80]

VCCGI

IccMax = 25 A CRB r1p0 p51, p52

22UF MLCC CAPACITORS PLACE AT POWER PAGE 46

Power Cap for +VCGI



VNN

IccMax = 4 A CRB 1r0p p51

22UF MLCC CAPACITORS PLACE AT POWER PAGE 47

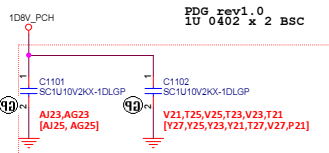
Power Cap for +VNN



1D05V_PCH O--> 1D05V_PCH [7]
 1D2V_VDDQ_S3 O--> 1D2V_VDDQ_S3 [7,12,13,45,48,64,80]
 1D8V_PCH O--> 1D8V_PCH [7]
 1P2V_DSI O--> 1P2V_DSI [7]
 1P2V_GLML O--> 1P2V_GLML [7]
 1P2V_MPHY O--> 1P2V_MPHY [7]
 1P2V_PLL O--> 1P2V_PLL [7]
 1P2V_USB2 O--> 1P2V_USB2 [7]
 3D3V_S5 O--> 3D3V_S5 [7,16,17,18,19,24,31,36,37,39,41,42,45,61,63,65,95,96,99]
 RTC_AUX_S5 O--> RTC_AUX_S5 [7,18,24,25,27]
 VCCIOA O--> VCCIOA [7]

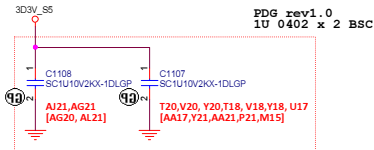
CRB r1p0 p52

+VDD1_1P8



1UF*2 placed at back side of package(Bottom side)

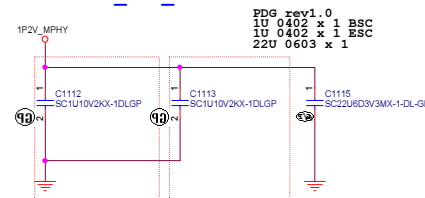
+VDD3_3P3



1UF*2 placed at back side of package(Bottom side)

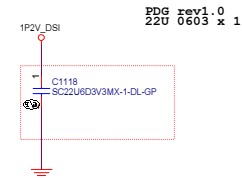
CRB r1p0 p53

+VDD2_1P2_MPHY



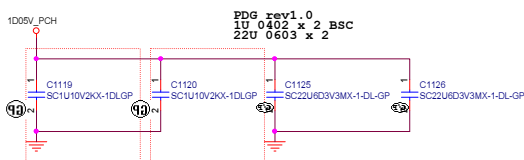
1UF*1 placed at back side of package(Bottom side)
 1UF*1 placed at edge side of package(Top side)
 22UF*1 placed between BGA and VR

+VDD2_1P2_DSI



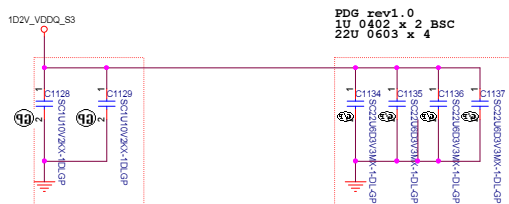
22UF*1 placed between BGA and VR

+VCCRAM_1P05_VCCRAMIO



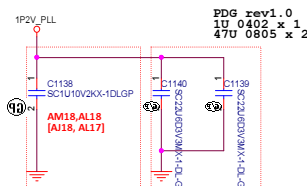
1UF*2 placed at back side of package(Bottom side)
 22UF*2 placed between BGA and VR

+VCCDDQ



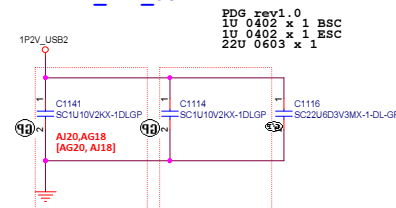
1UF*2 placed at back side of package(Bottom side)
 22UF*4 placed between BGA and VR

+VDD2_1P2_PLL



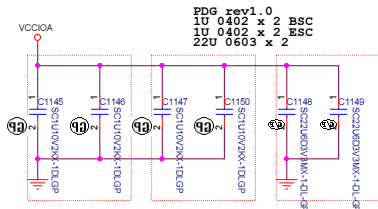
1UF*1 placed at back side of package(Bottom side)
 22UF*2 placed between BGA and VR

+VDD2_1P2_USB2



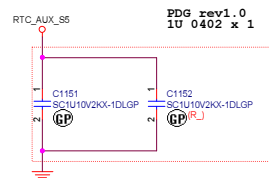
1UF*1 placed at back side of package(Bottom side)
 1UF*1 placed at edge side of package(Top side)
 22UF*1 placed between BGA and VR

+VCCIOA



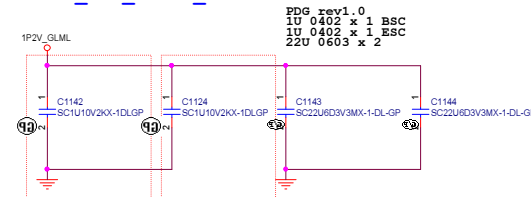
1UF*2 placed at back side of package(Bottom side)
 1UF*2 placed at edge side of package(Top side)
 22UF*2 placed between BGA and VR

+VCCRTC_3P3



1UF*2 placed at edge side of package(Top side)

+VDD2_1P2_GLML2_HPLDO

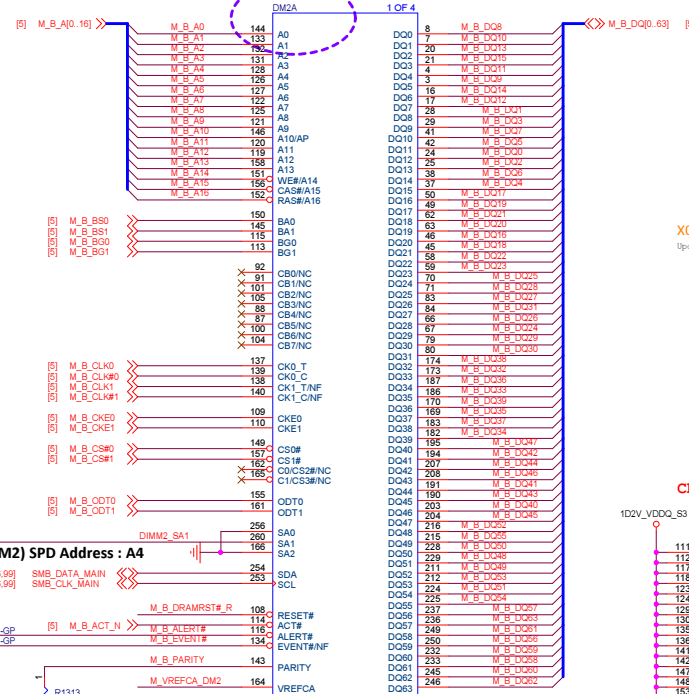
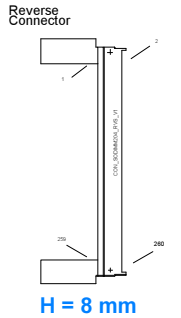


1UF*1 placed at back side of package(Bottom side)
 1UF*1 placed at edge side of package(Top side)
 22UF*2 placed between BGA and VR

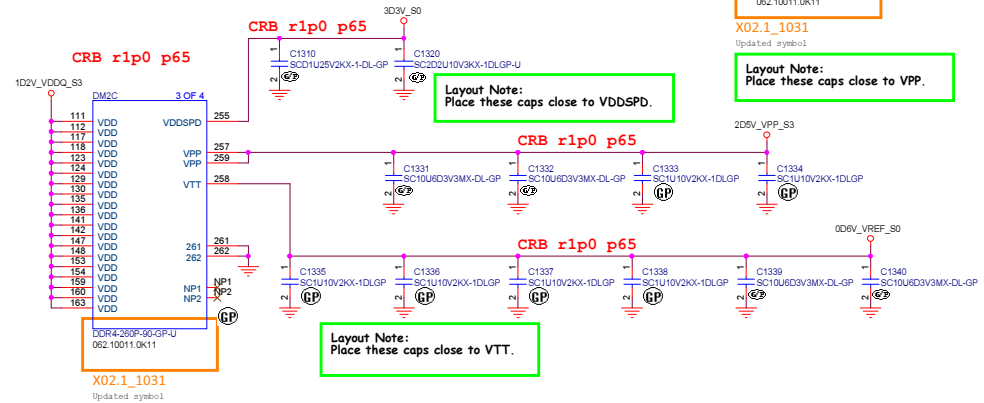
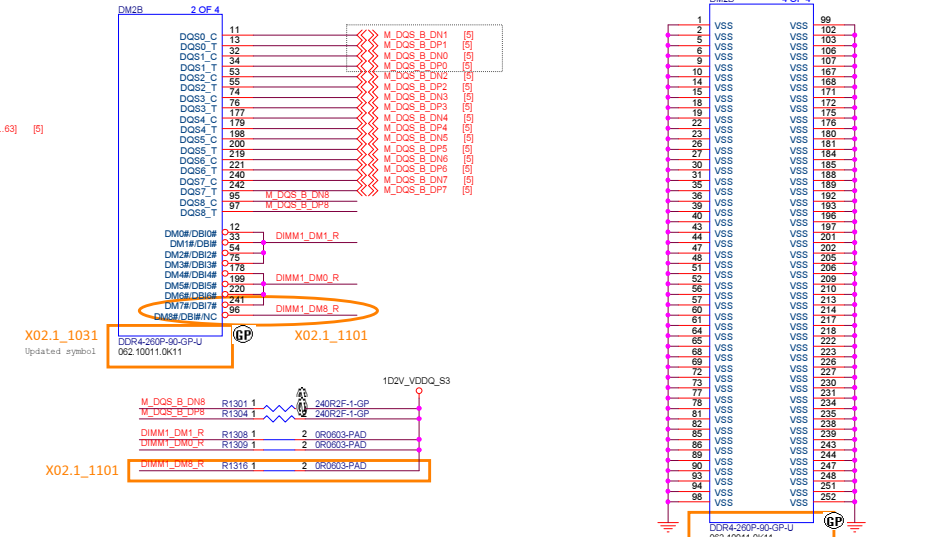
CRB r1p0 p64

New part: ASAA827-E8RB0-7H
Need to update symbol & PN

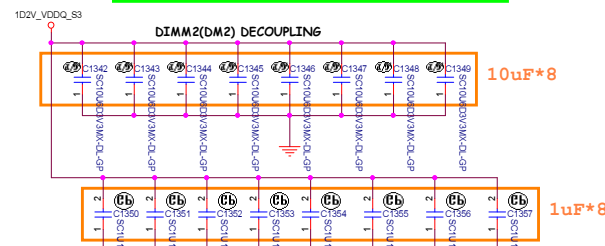
Channel 1
DIMM2(DM2)



2nd source:
062.10011.0K61



Layout Note:
Place these Caps near DIMM2(DM2).
4 near each side of the DIMM connector close to VDD pins



SPD Address Table

SMBus 0			
Device	8-bit Address(hex)		
DIMM A0	Read Addr:0xa2	SA1=0; SA0=0	
	Write Addr:0xa1		
DIMM A1	Write Addr:0xa2	SA1=0; SA0=1	
	Read Addr:0xa3		
DIMM B0	Write Addr:0xa4	SA1=1; SA0=0	
	Read Addr:0xa5		
DIMM B1	Write Addr:0xa6	SA1=1; SA0=1	
	Read Addr:0xa7		
1	0	1	0
SA1	SA0		

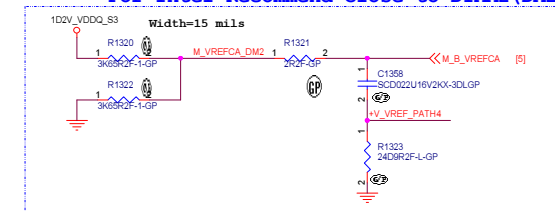
Note: 0' 3~7 bit as default

```
PDG: r1p0
VTT: 10U 0603 x 2
VDD: 0.1U 0402 x 2, 10U 0603 x 8, 1U 0402 x 8
```

For Intel Recommend Close to DIMM2 (DM2)



For Intel Recommend Close to DIMM2 (DM2)



Blanking

1DRV_S5 -> 1DRV_S5 [7,8,16,17,18,19,21,24,25,37,39,45,61,63,65,91,99]

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

EDS r1p0:
All the straps are sampled at Rising Edge of RSM_RST_N

GPIO

Circuit

High

Low

Circuit

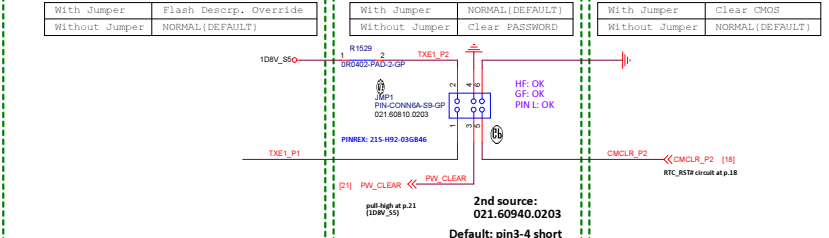
High

Low

FLASH DESCRIPTOR OVERRIDE

PASSWORD CLEAR

CLEAR CMOS



PCB Silkscreen follow Behavioral Spec

Jumper	Function	Label	Operation
JMP1	SERVICE_MODE	SERVICE_M	1 - 2 Short : Disable 1 - 2 Open : Default
	PASSWORD	PW_CLR	3 - 4 Short : Default 3 - 4 Open : Clear
	CMOS	COMS	5 - 6 Short : Clear 5 - 6 Open : Default

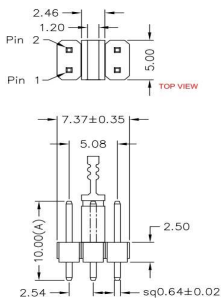


Table 2-28. Hardware Straps (Sheet 2 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) Note: The board should strap this low and do not use otherwise
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FSD	RSVD	20K PD	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_85	SIO_SPI_2_FSD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SY	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) Note: Platforms should strap this LOW. Functionality is handled by the PMC.

Table 2-28. Hardware Straps (Sheet 1 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable Note: This strap enables the platform to override security features in the SPI.
GPIO_42	MDS1_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_43	MDS1_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Note: This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Notes: 1. DNX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.

Table 2-28. Hardware Straps (Sheet 3 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BR1_DT	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_192	CNV_BR1_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

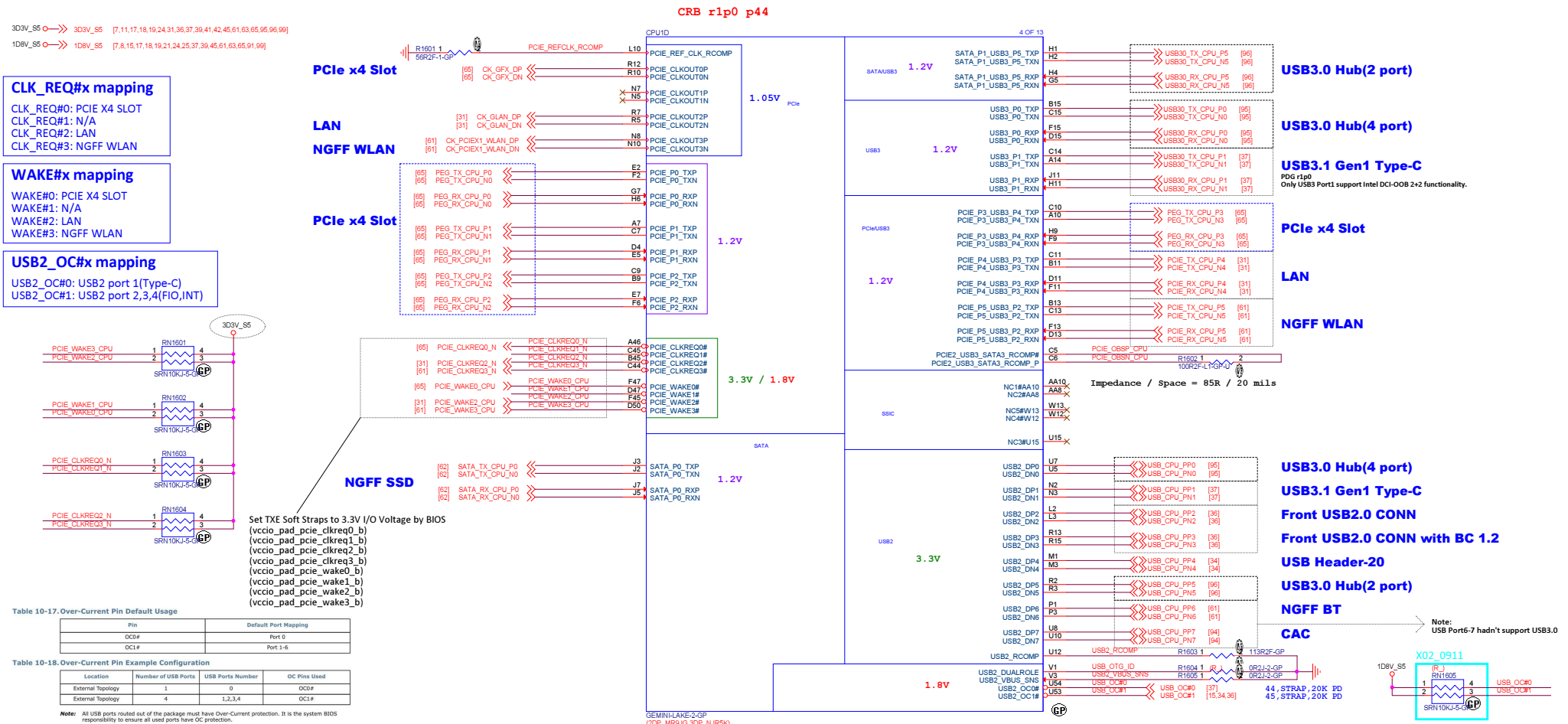


Figure 3-2. USB 2.0 and USB 3.0 Port Mapping

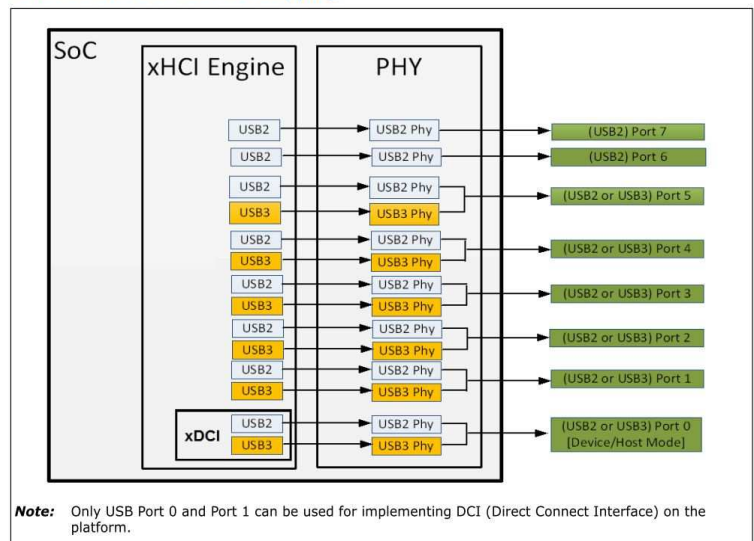
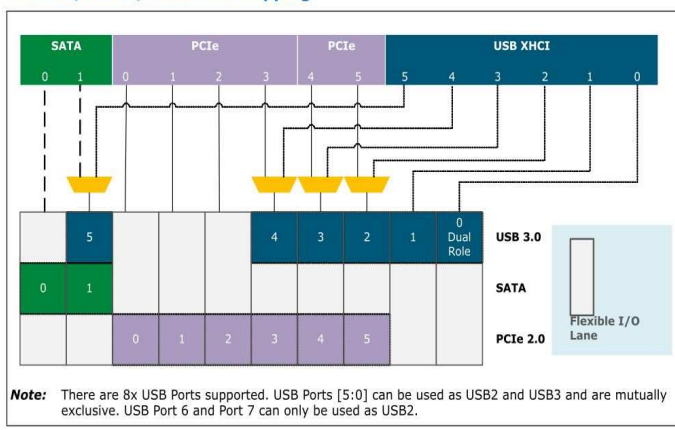


Figure 3-1. USB 3.0/PCIe*/SATA Port Mapping



When the platform does not use the USB2_OTG_ID, USB2_VBUS_SNS, and USB2_OC0/I, N pins:
 • USB2_OTG_ID and USB2_OC0/I, N pins can be left unconnected.
 • USB2_VBUS_SNS needs to be connected to GND.
 The USB2_OTG_ID pin has an internal 100kohm pull up and the USB2_OC0/I, N pins have an internal 20K pull up, so an external pull up is not required. However, if customers are concerned on platform EMI, it is recommended to use external 10K pull up resistor to V1P8A.



To configure the I²C ports, follow the pin muxing options listed out in the Gemini Lake SoC - External Design Specification (EDS).

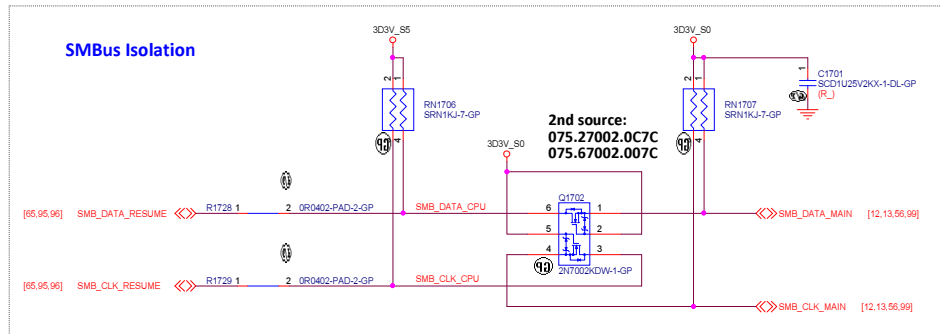


[8,58] DP2_HPD >>

DP2_CBL_DET_N
H: No detect (1.8V)
L: Detect

2nd source:
075.27002.0C
075.67002.00

DP1_CBL_DET_N
H: No detect (1.8V)
L: Detect



X02 0909



Board ID Settings

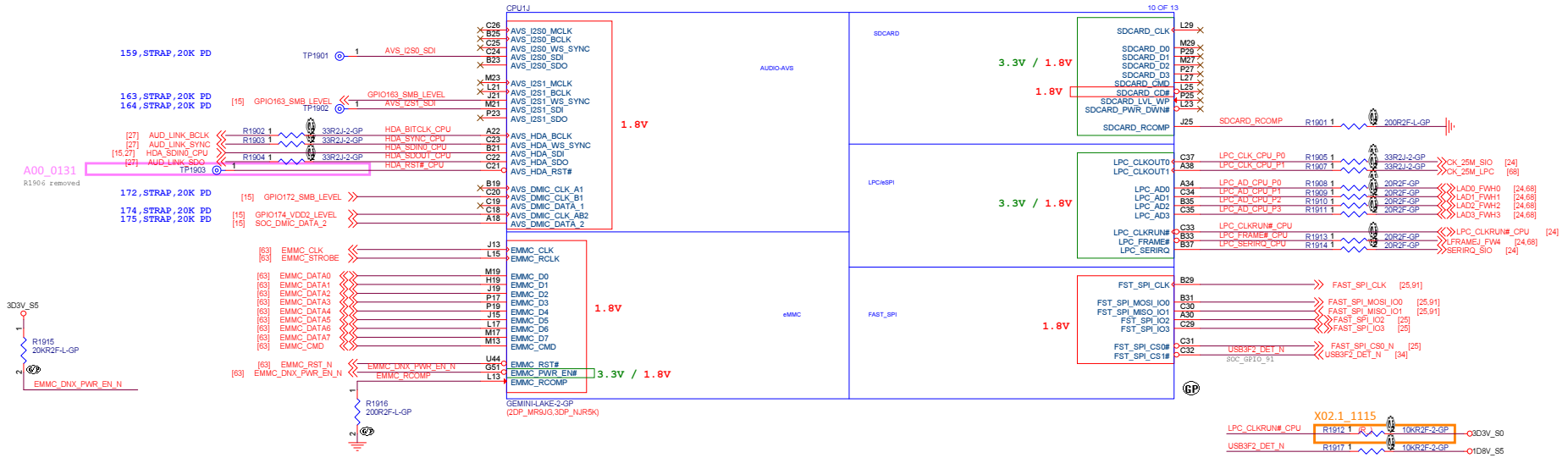
MB Version	Board2	Board1
X00 (EVT)	0V	0V
X01 (DVT1)	0V	0.9V
X02 (DVT2)	0V	1.8V
Reserve	0.9V	1.8V
A00 (PVT)	1.8V	1.8V



X02 0824

3D3V_S0 0 → 3D3V_S0 [12,13,17,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]
 3D3V_S5 0 → 3D3V_S5 [7,11,16,17,18,24,31,36,37,39,41,42,45,61,63,65,95,96,99]
 1D8V_S5 0 → 1D8V_S5 [7,8,15,16,17,18,21,24,25,37,39,45,61,63,65,91,99]

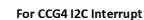
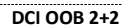
CRB r1p0 p42



PDG r1p0

1. For B-step silicon, EMMC_RST_N will have an internal pull up of 20K and an external pull-up is not needed on the platform.

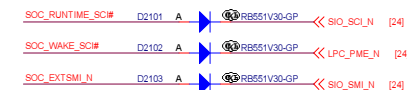
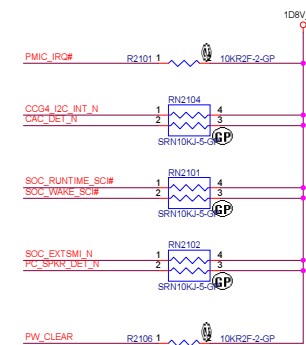
Blanking



```
27,STRAP,20K PU
28,STRAP,20K PU
```

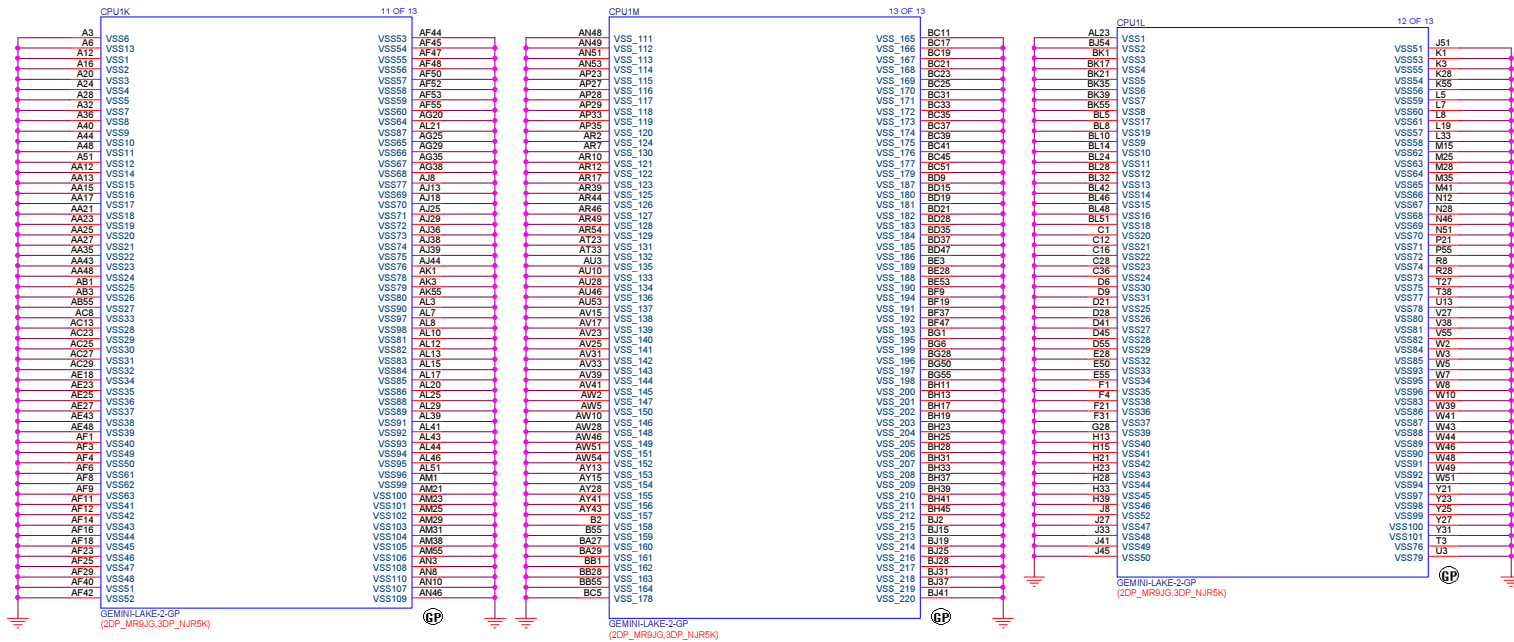
Set TXE Soft Straps to 3.3V I/O Voltage by BIOS
(vccio_pad_gpio_134=0)
(vccio_pad_gpio_135=0)
(vccio_pad_gpio_136=0)
(vccio_pad_gpio_137=0)

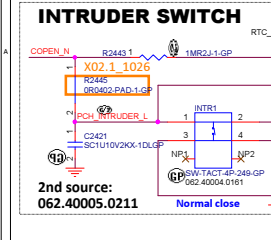
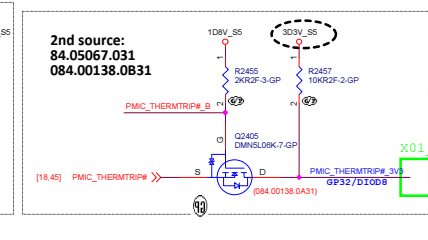
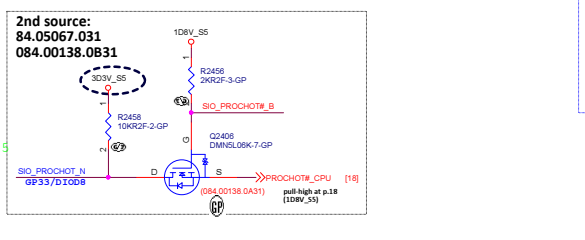
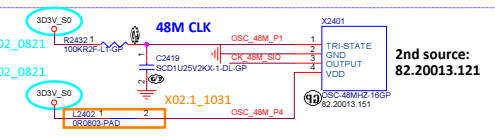
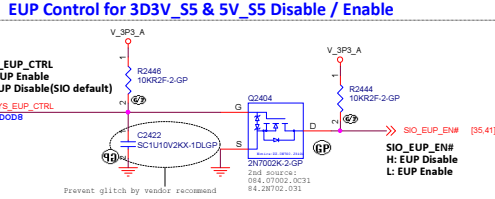
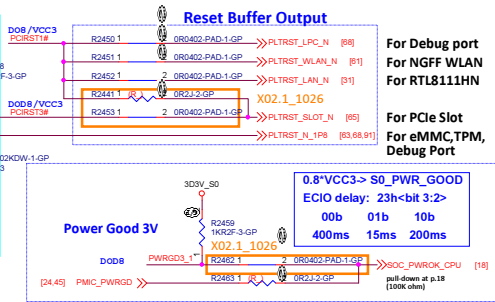
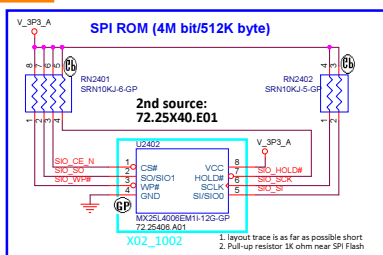
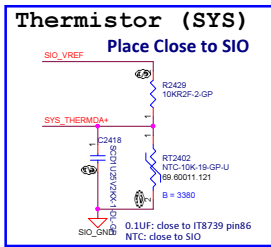
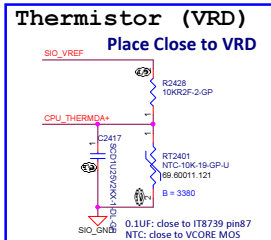
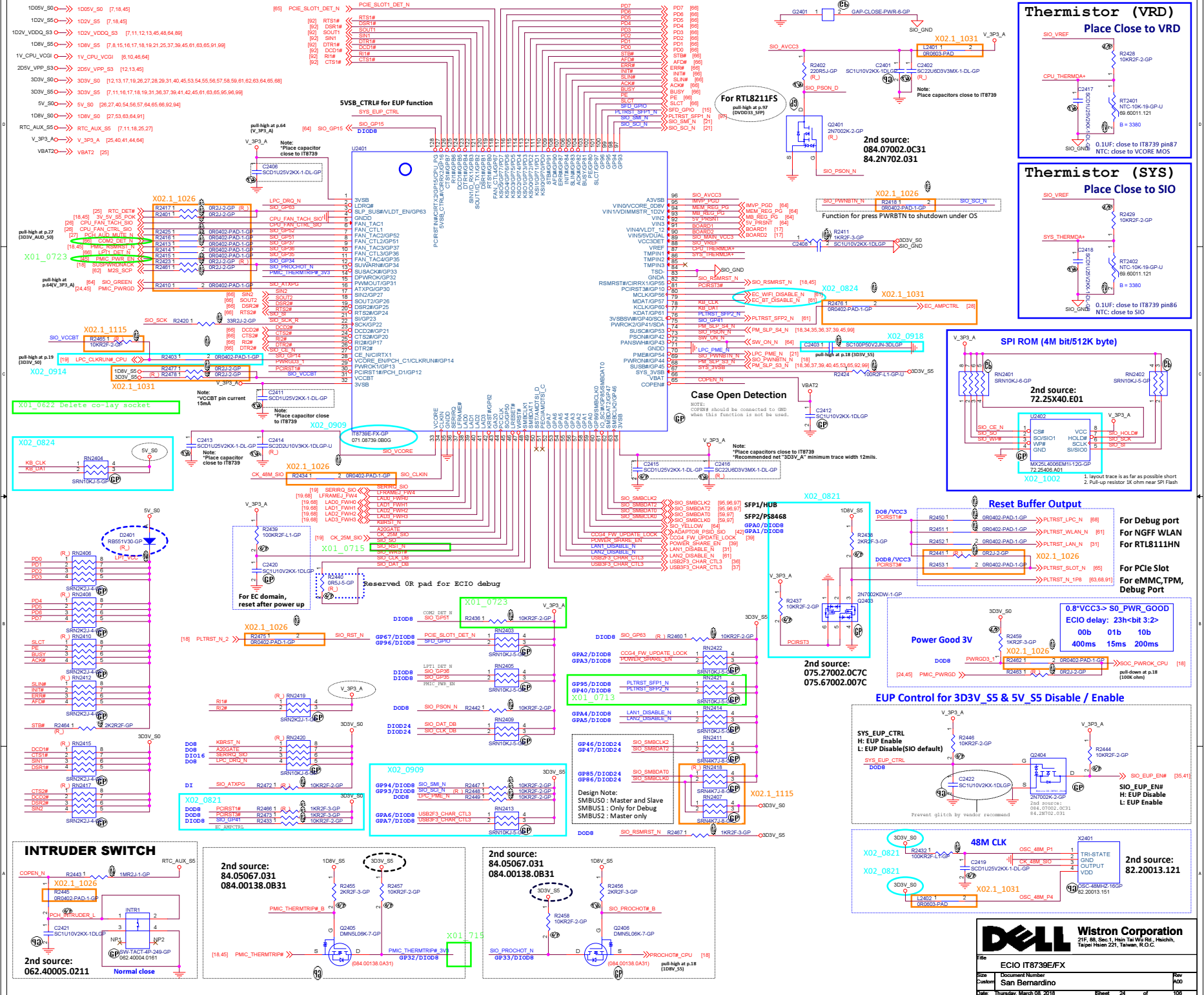
Set TXE Soft Straps to 3.3V I/O Voltage by BIOS
(vccio pad gpio 142=0)



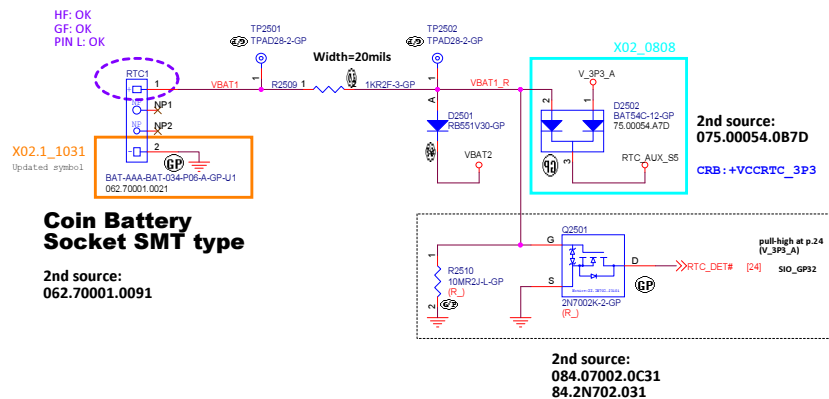
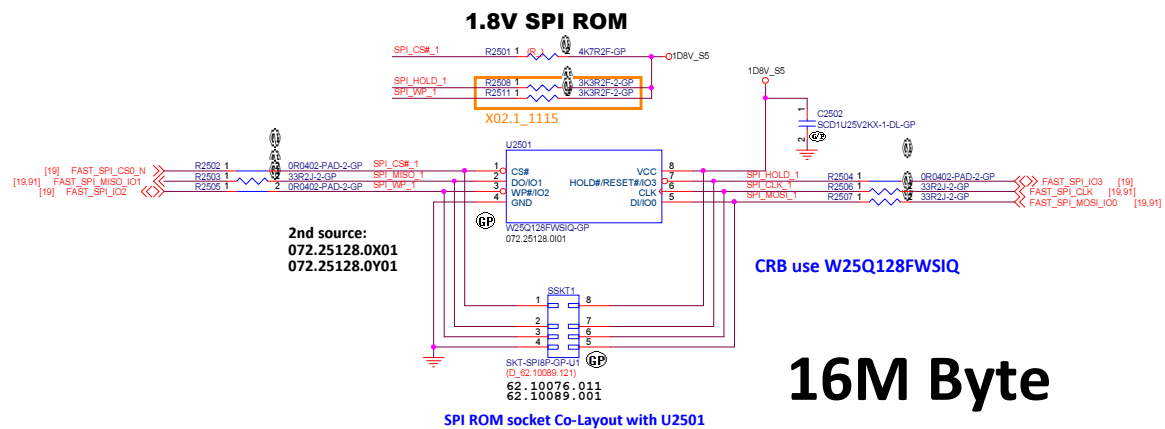
Blanking

CRB r1p0 p48





1D8V_S5 0--> 1D8V_S5 [7,8,15,16,17,18,19,21,24,37,39,45,61,63,65,91,99]
 RTC_AUX_S5 0--> RTC_AUX_S5 [7,11,18,24,27]
 V_3P3_A 0--> V_3P3_A [24,40,41,44,64]
 VBAT2 0--> VBAT2 [24]

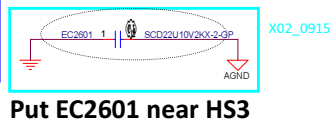
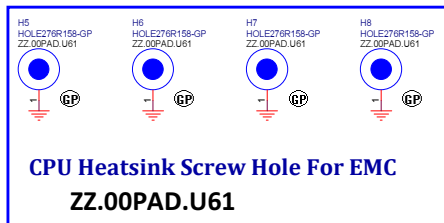
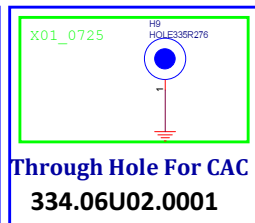
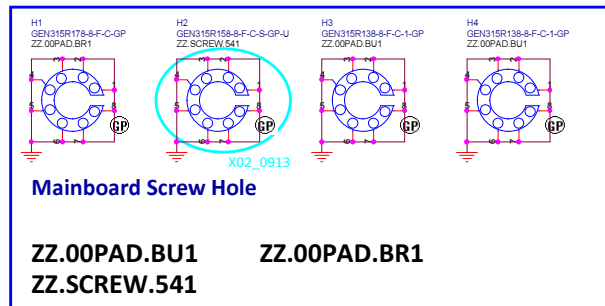
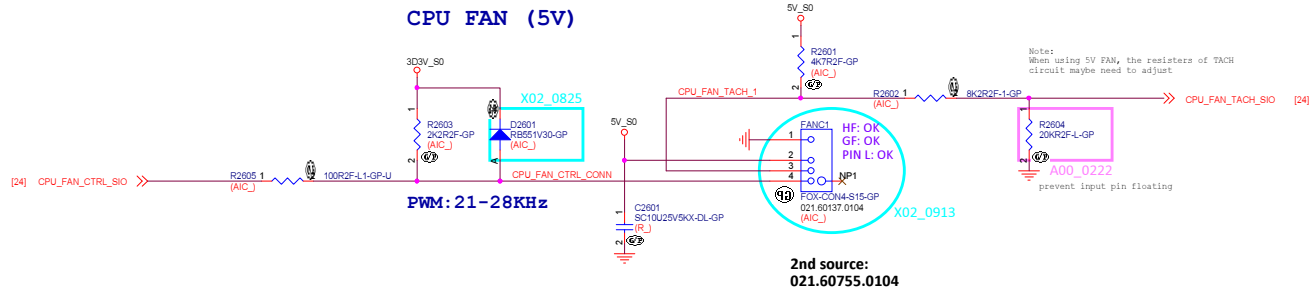


Battery (CR2032):
 23.22063.001



2nd source:
 23.20068.001
 23.21012.001
 23.20023.311

3D3V_S0 → 3D3V_S0 [12,13,17,19,24,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]
 5V_S0 → 5V_S0 [24,27,40,54,56,57,64,65,66,92,94]
 AGND → AGND [27,28,29,89]



For 6L PCB
 -1(A00)
 WWVX3\$JA GCE
 WWVX3\$KA TRIPOD
 WWVX3\$CA HANNSTAR
 WWVX3\$LA TPT



40.3NH24.011



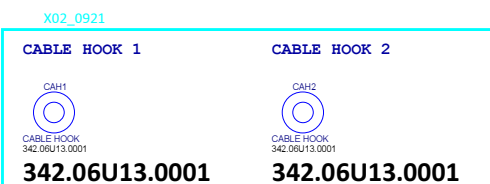
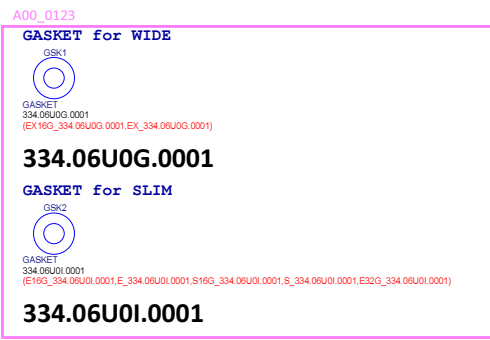
45.3E702.001



360.06U02.0001
360.06U02.0011



38.02007.001
38.02007.011

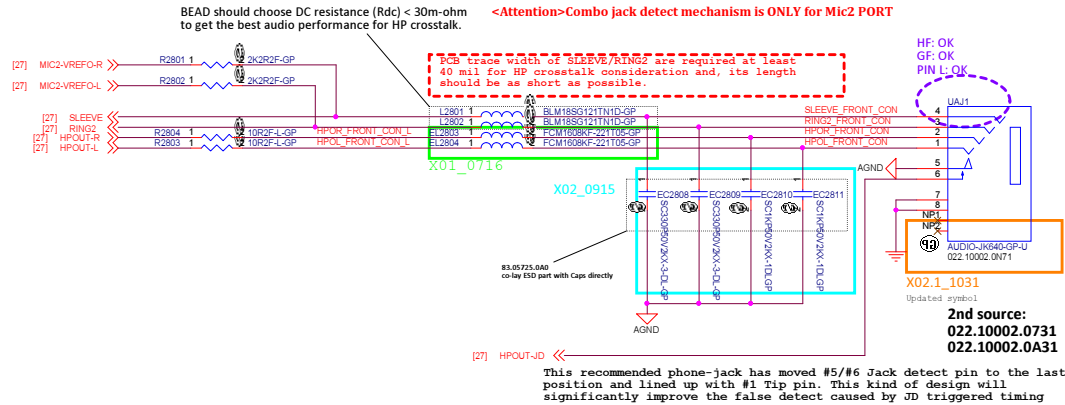


AGND [26,27,28,89]
V_5P0_A [27,34,35,36,37,39,40,41,44,45,46,48,89,92]
3D3V_SD [12,13,17,19,24,26,27,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]

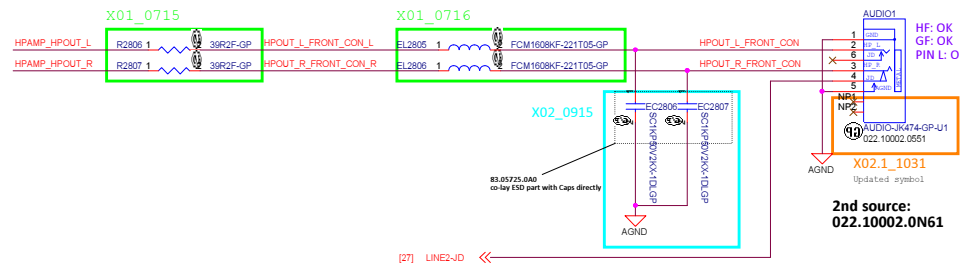
Global Headset Jack 1 for Front

OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

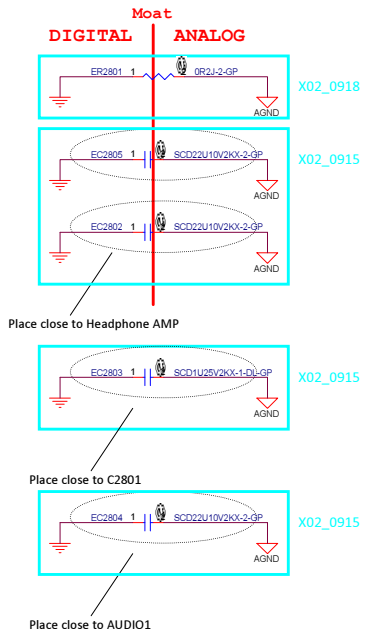
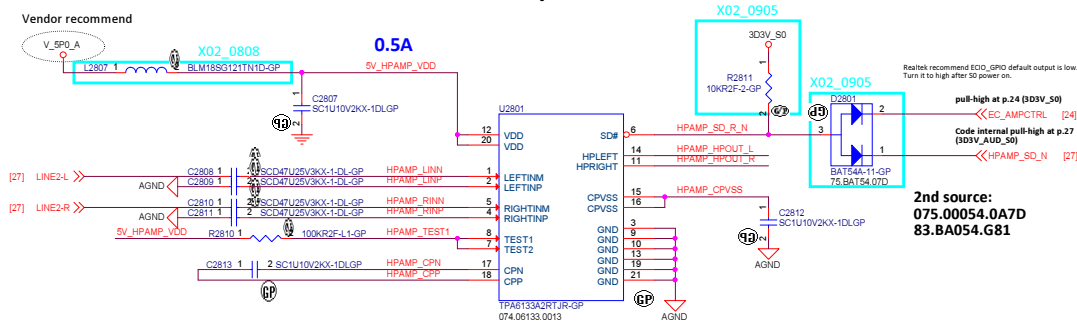
<Attention>Combo jack detect mechanism is ONLY for Mic2 PORT



Front Headphone

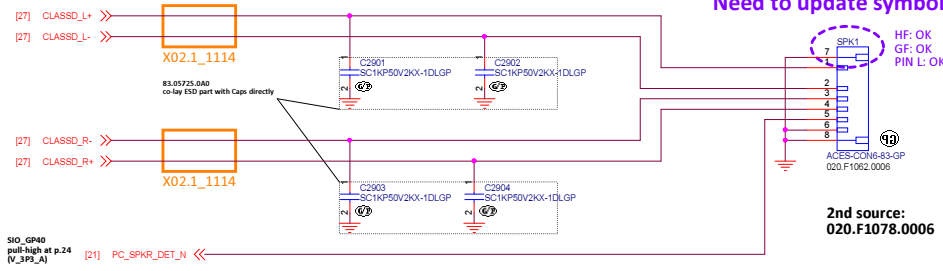


Headphone AMP



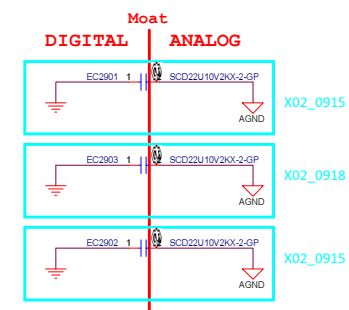
AGND [26,27,28,89]
 3D3V_S0 [12,13,17,19,24,26,27,28,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]

Trace width for SPK-L+ / SPK-L- / SPK-R+ / SPK-R-
 Speaker 2W/4 ohm : 40 mil
 Speaker 2W/8 ohm : 20 mil



INTERNAL SPEAKER

New part: 50273-00671-001
 Need to update symbol & PN

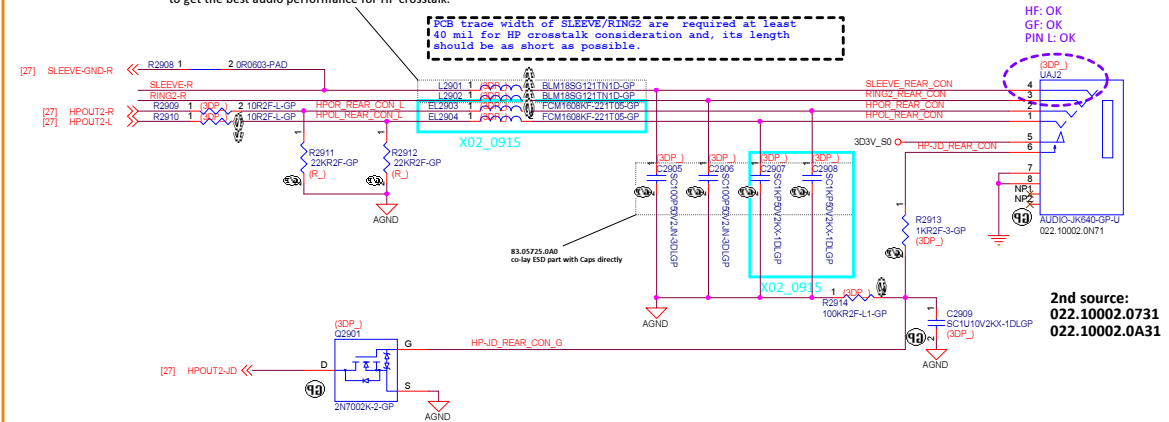


X02.1_1120

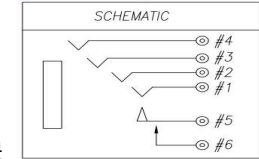
Global Headset Jack 2 for Rear side

BEAD should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.
 OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

For trace width of SLEEVE/RING2 are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.



Pin Define:
 Pin1:HP_L
 Pin2:HP_R
 Pin3:Ring2
 Pin4:Sleeve
 Pin5:AGND
 Pin6:JD
 Pin7:GND
 Pin8:GND



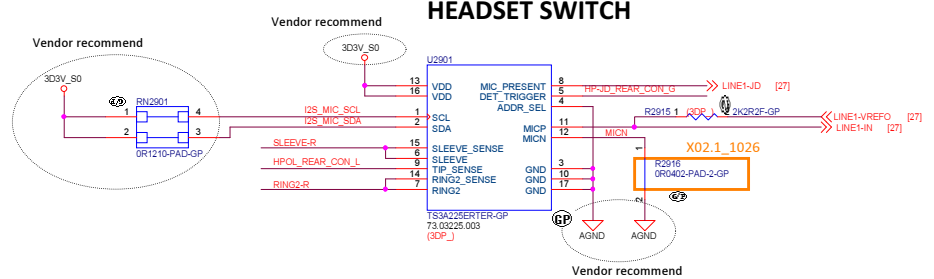
4-pin 3.5mm Headset Connector Pinout





Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Microphone
4	Sleeve	Ground / Common

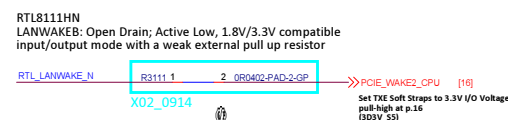
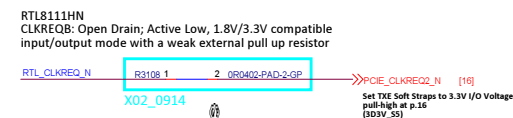
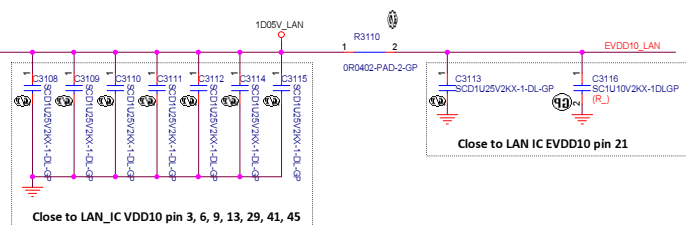
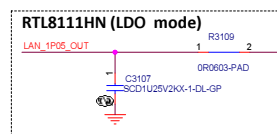
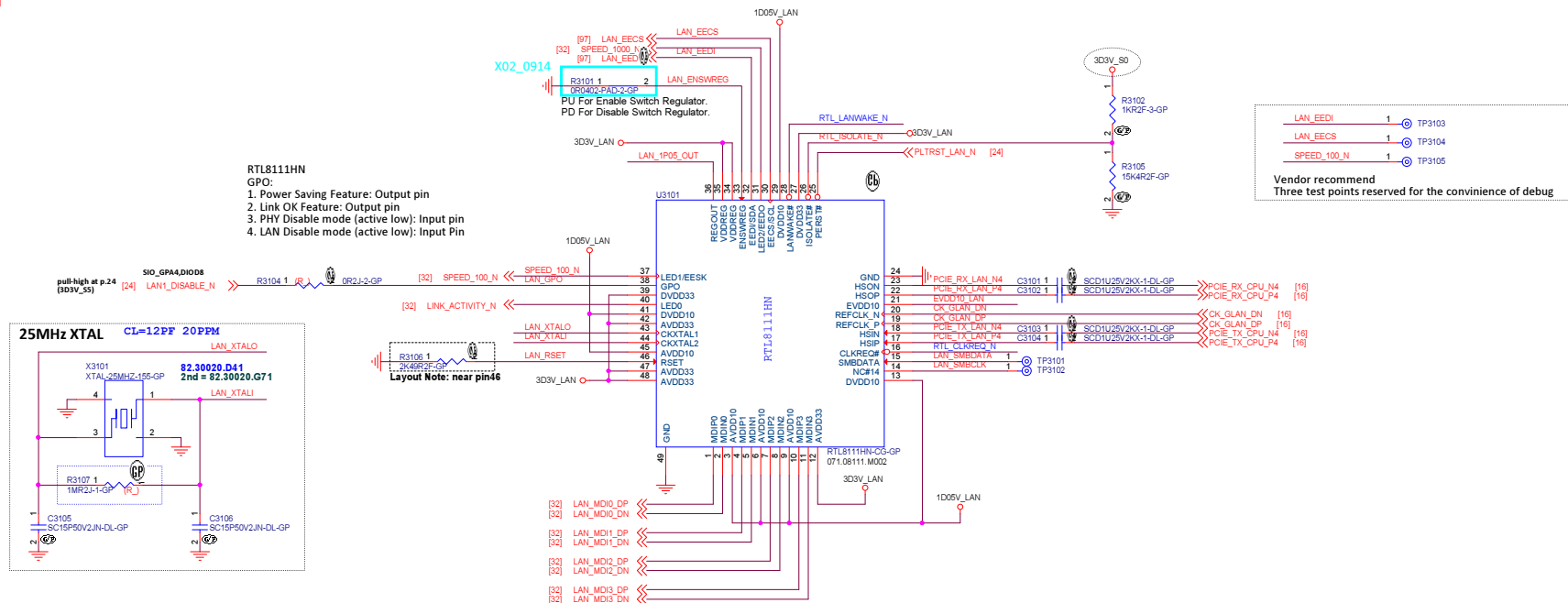
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Ground / Common
4	Sleeve	Microphone

HEADSET SWITCH

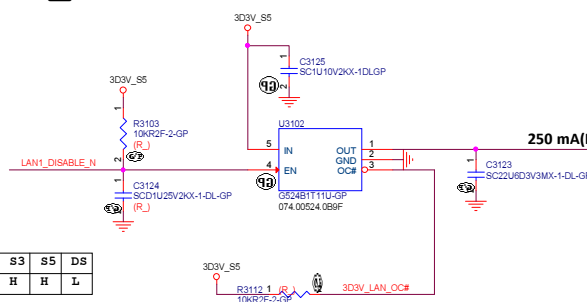


Blanking

3D3V_S0		3D3V_S0	[12,13,17,19,24,26,27,28,29,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]
3D3V_S5		3D3V_S5	[7,11,16,17,18,19,24,36,37,39,41,42,45,61,63,65,95,96,99]
3D3V_LAN		3D3V_LAN	[32,97]

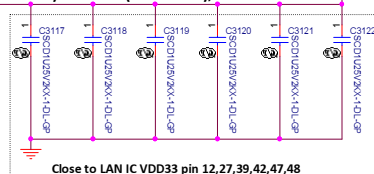


3D3V LAN Switch



Note:
Rising time (10%~90%) have to $>0.5\text{ms}$ and $<100\text{ms}$

250 mA(RTL8111HN) + 150 mA(RTL8211FS), 40 mils width

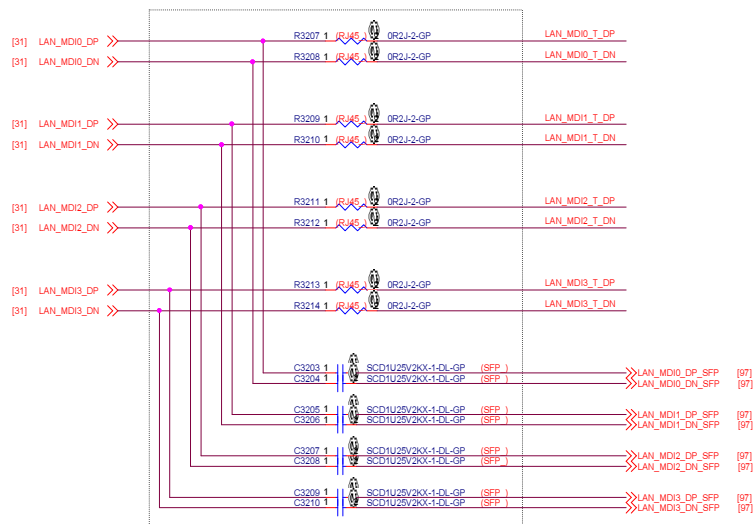


Icc33	Average Operating Supply Current from 3.3V (does NOT include 1.0V power consumption)	At 1Gbps with heavy network traffic	-	65	-	mA
Icc10	Average Operating Supply Current from 1.0V	At 1Gbps with heavy network traffic	-	150	-	mA
Isys33	Average Operating Supply Current for total system 3.3V (includes 1.0V power consumption)	At 1Gbps with heavy network traffic	-	Note3	-	mA

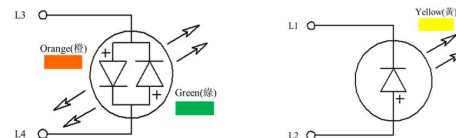
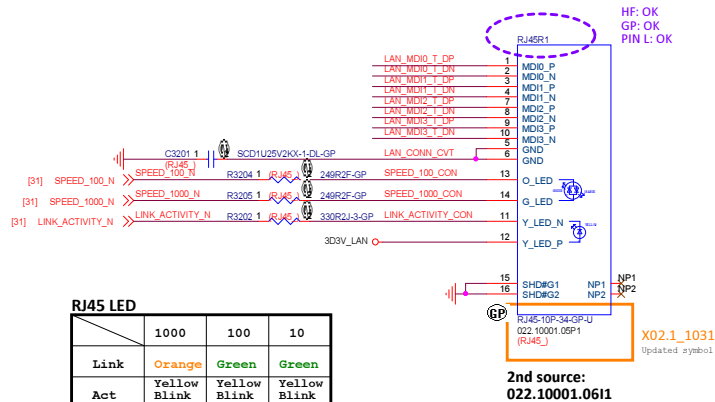
Note 1: Refer to the latest schematic circuit for correct configuration.
 Note 2: All Supply Mean Voltage power noise $\leq \pm 5\%$ of Mean Voltage.
 Note 3: The total operating current $I_{s33} = I_{cc33} + (I_{cc10} / \text{efficiency} / 3.3)$,
 Where efficiency = 0.75 for SWR-mode or efficiency = 0.33 for LDO-mode.

3D3V_LAN >>> 3D3V_LAN [31,97]
3D3V_SS >>> 3D3V_SS [7,11,16,17,18,19,24,31,36,37,39,41,42,45,61,63,65,66,96,99]

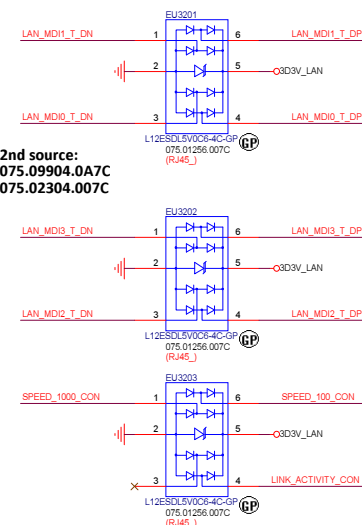
Co-layout for either RJ45 or SFP SKU



RJ45R1

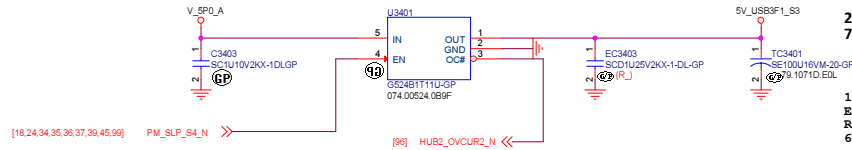
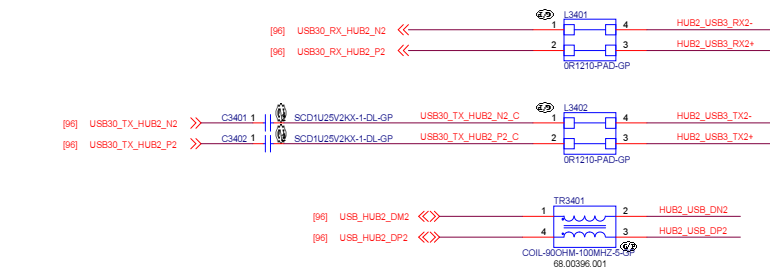


ESD



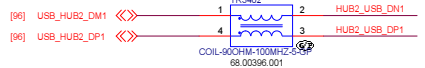
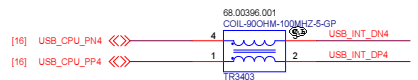
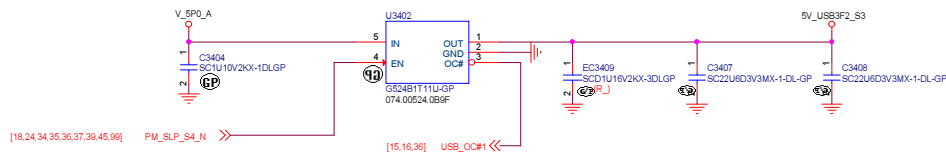
Blanking

V_5P0_A O--> V_5P0_A [27,28,35,36,37,39,40,41,44,45,46,48,89,92]



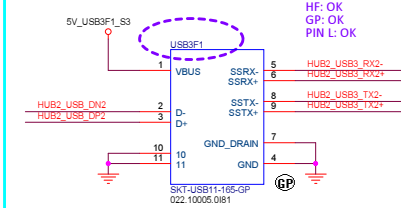
2nd source:
77.51071.02L

100uF/16V,
ESR=23.0mohm,
Ripple Current= 2490 mA
6.3*6 SOLID CAP



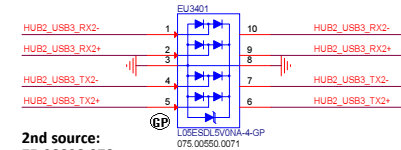
X02_0904

FRONT - USB3F1

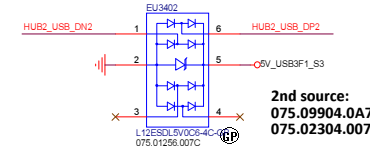


2nd source:
022.10005.0AK1
022.10005.0AM1

ESD

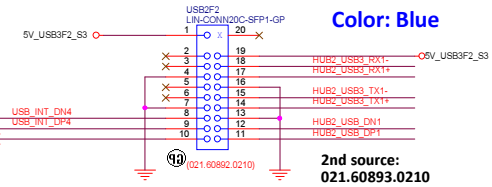


2nd source:
75.08808.073
075.01043.0073



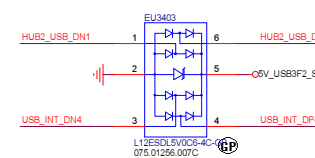
2nd source:
075.09904.0A7C
075.02304.007C

Internal USB3.0 Header-20



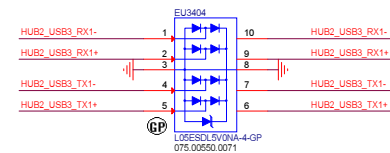
2nd source:
021.60893.0210

ESD



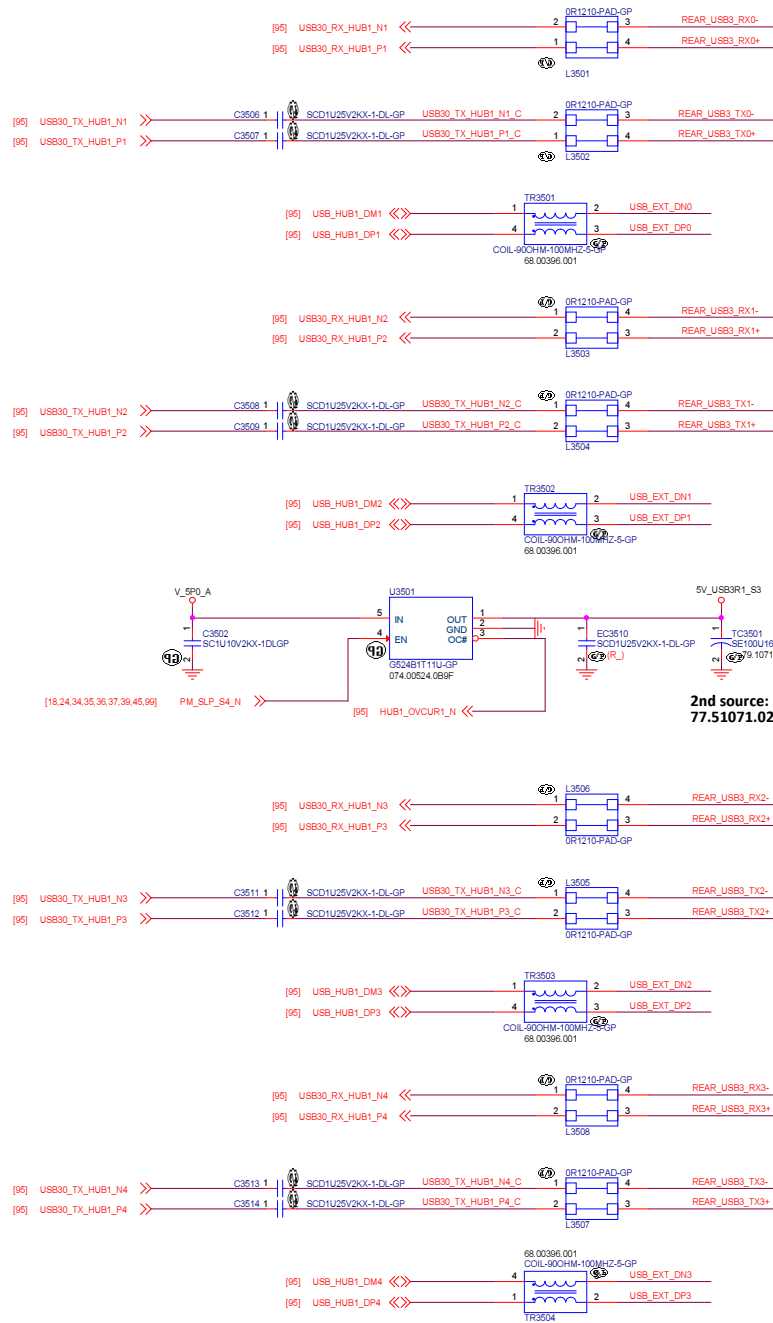
2nd source:
075.09904.0A7C
075.02304.0C7C

ESD



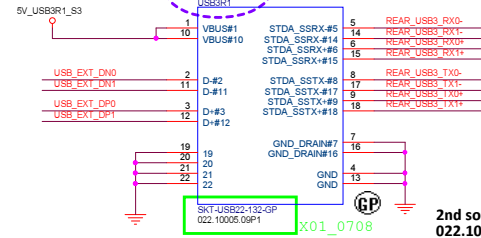
2nd source:
75.08808.073
075.01043.0073

V_5P0_A >> V_5P0_A [27,28,34,36,37,39,40,41,44,45,46,48,89,92]

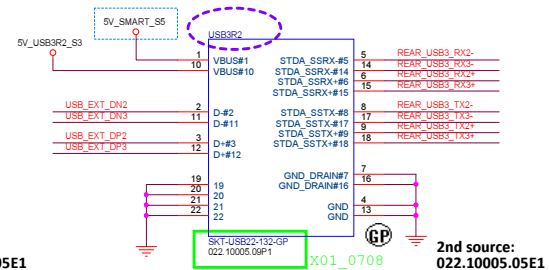


HF: OK
GP: OK
PIN L: OK

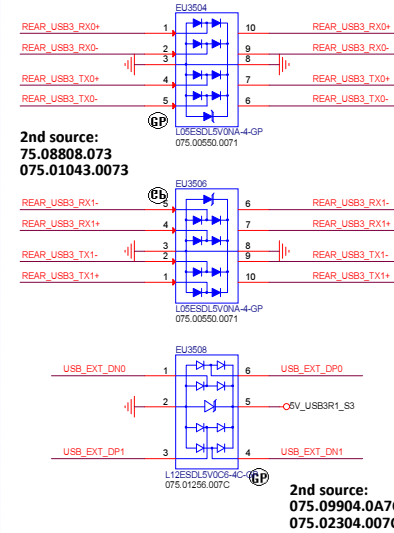
REAR USB3R1



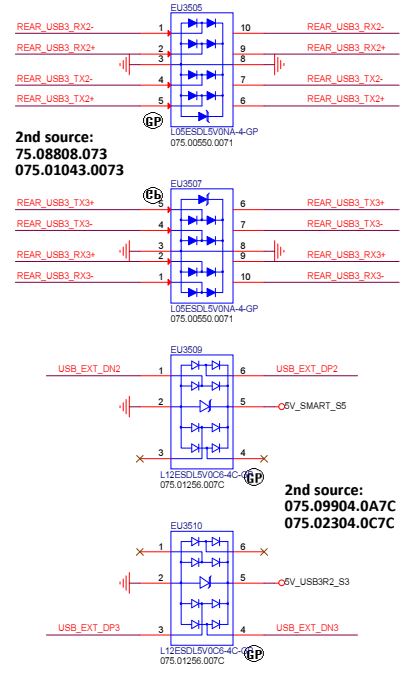
REAR USB3R2



ESD



ESD



HF: OK
GP: OK
PIN L: OK

2nd source: 77.51071.02L

100uF/16V,
ESR=23.0mohm,
Ripple Current= 2490 mA
6.3*6 SOLID CAP

2nd source: 022.10005.05E1

100uF/16V,
ESR=23.0mohm,
Ripple Current= 2490 mA
6.3*6 SOLID CAP

2nd source: 77.51071.02L

100uF/16V,
ESR=23.0mohm,
Ripple Current= 2490 mA
6.3*6 SOLID CAP

2nd source: 022.10005.05E1

100uF/16V,
ESR=23.0mohm,
Ripple Current= 2490 mA
6.3*6 SOLID CAP

2nd source: 77.51071.02L

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

Title		
Rear USB3.0 Stack		
Doc No	Document Number	Rev
C	San Bernardino	000
Date	Thursday, March 08, 2018	Sheet 35 of 106

303V_S5 -> 303V_S5 [7,11,16,17,18,19,24,31,36,39,41,42,45,61,63,65,95,96,99]
 108V_S5 -> 108V_S5 [7,15,16,17,18,19,21,24,25,36,45,61,63,65,91,99]
 V_5P0_A -> V_5P0_A [27,28,34,36,39,40,41,44,45,46,48,89,92]
 5V_USB3F3_CHAR0 -> 5V_USB3F3_CHAR [39]

For DisplayPort differential signal trace length:

PS8468

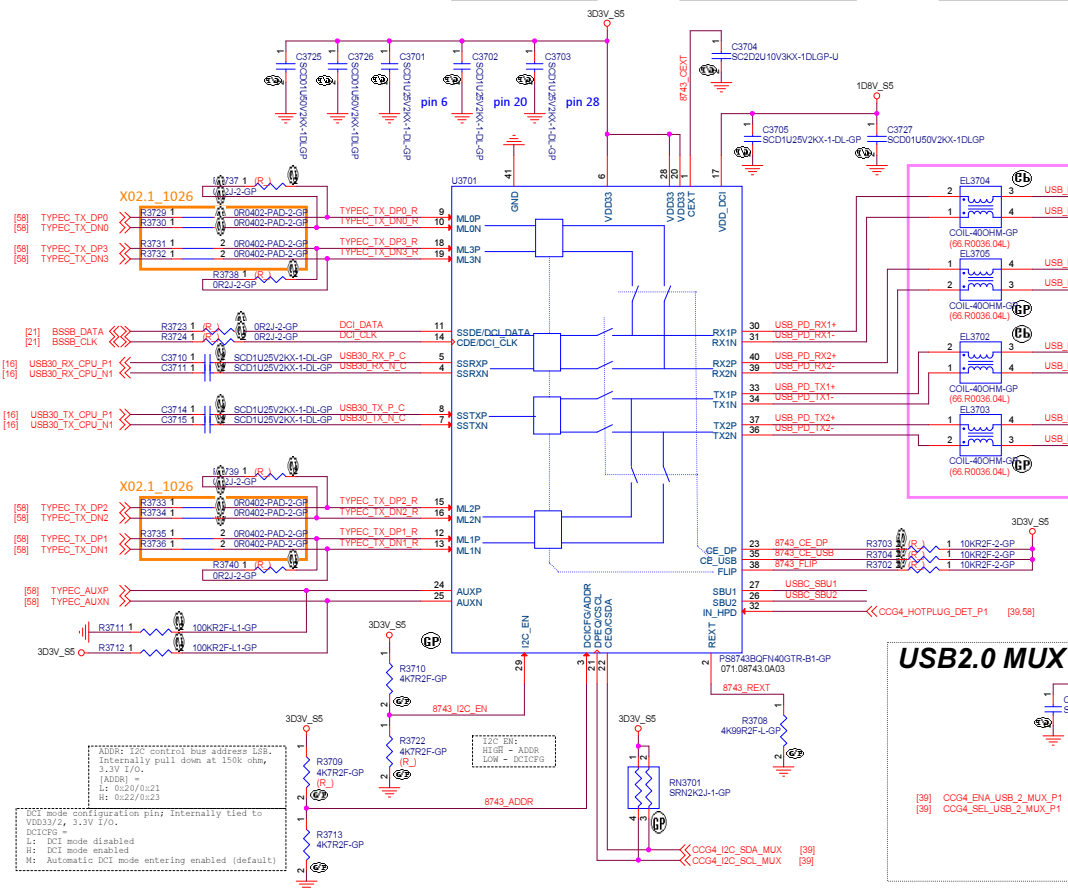
> 6"

< 15"

PS8743B

2"

Type-C Connector



2nd source:
 009.1071D.0061
 100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

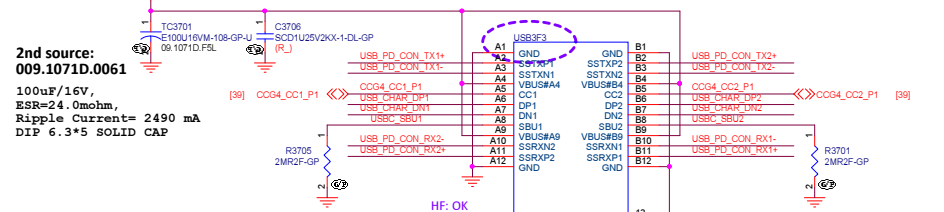
100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

100nF/16V,
 ESR=24.0mohm,
 Ripple Current= 2490 mA
 DIP 6.3*5 SOLID CAP

FRONT USB3.1 TYPE C



2nd source:
 062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

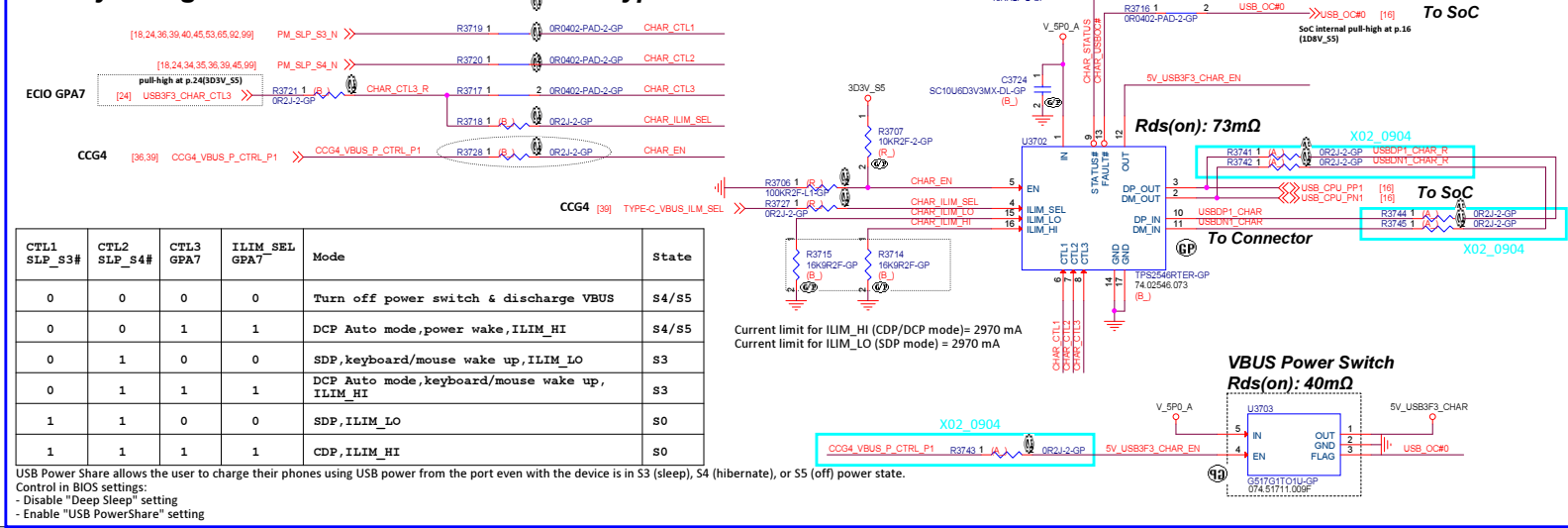
062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

062.10009.0B11
 062.10009.0D91

Battery Charger 1.2 IC - TI TPS2546 for Front Type-C



CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPA7	ILIM_SEL GPA7	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP Auto mode,power wake,ILIM_HI	S4/S5
0	1	0	0	SDP,keyboard/mouse wake up,ILIM_LO	S3
0	1	1	1	DCP Auto mode,keyboard/mouse wake up,ILIM_HI	S3
1	1	0	0	SDP,ILIM_LO	S0
1	1	1	1	CDP,ILIM_HI	S0

USB Power Share allows the user to charge their phones using USB power from the port even with the device in S3 (sleep), S4 (hibernate), or S5 (off) power state.

- Disable "Deep Sleep" setting
- Enable "USB PowerShare" setting

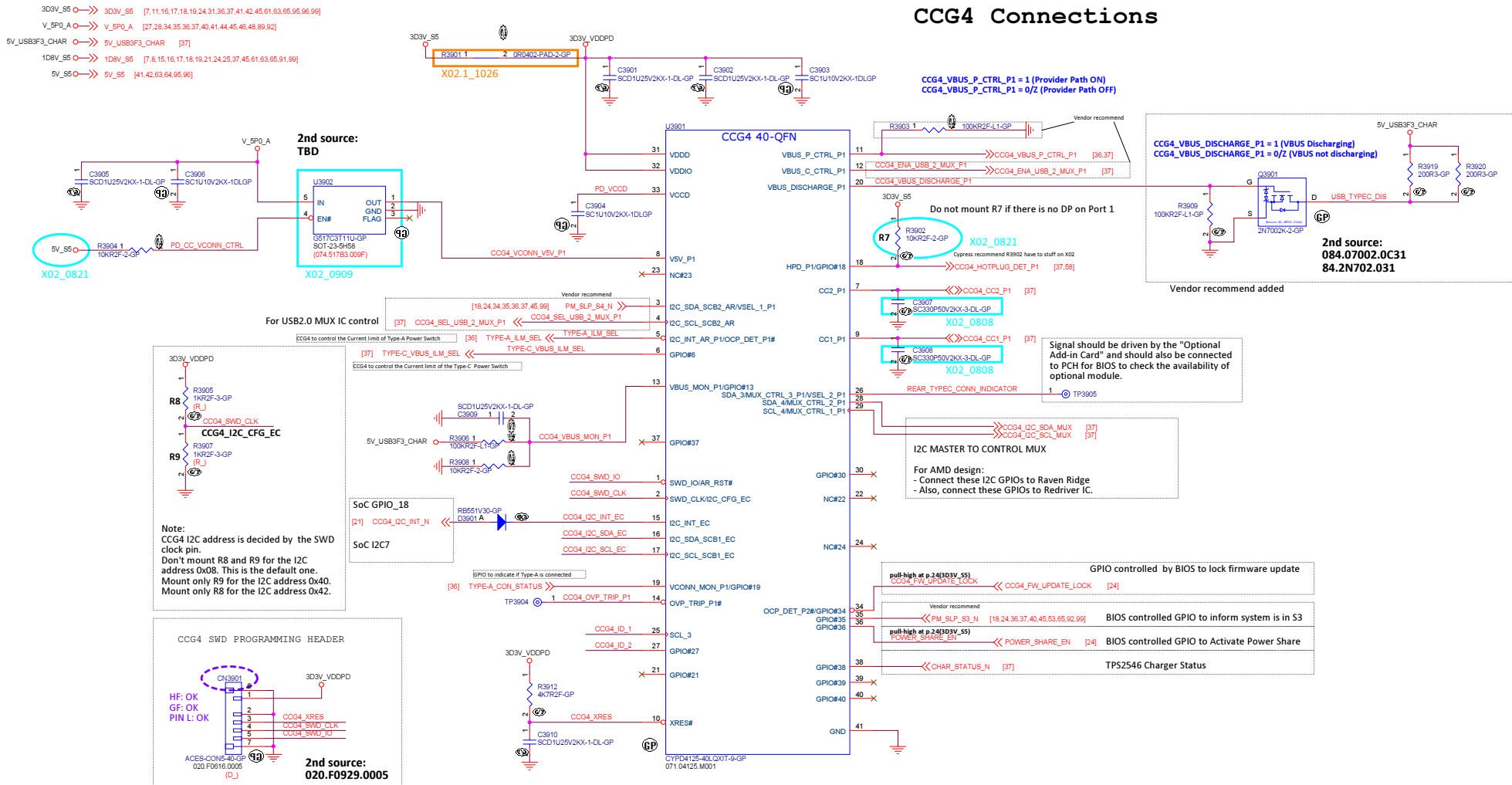
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsinchu 221, Taiwan, R.O.C.

Front TYPE-C
 Document Number
 San Bernardino
 Date: Thursday, March 08, 2018
 Sheet 37 of 106

Blanking

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taippei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size C	Document Number San Bernardino		Rev N00
Date: Thursday, March 08, 2018		Sheet 38 of	106

CCG4 Connections

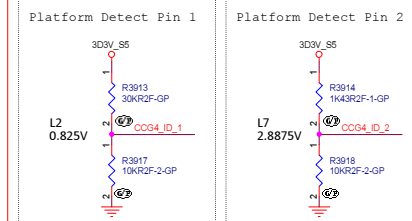


Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

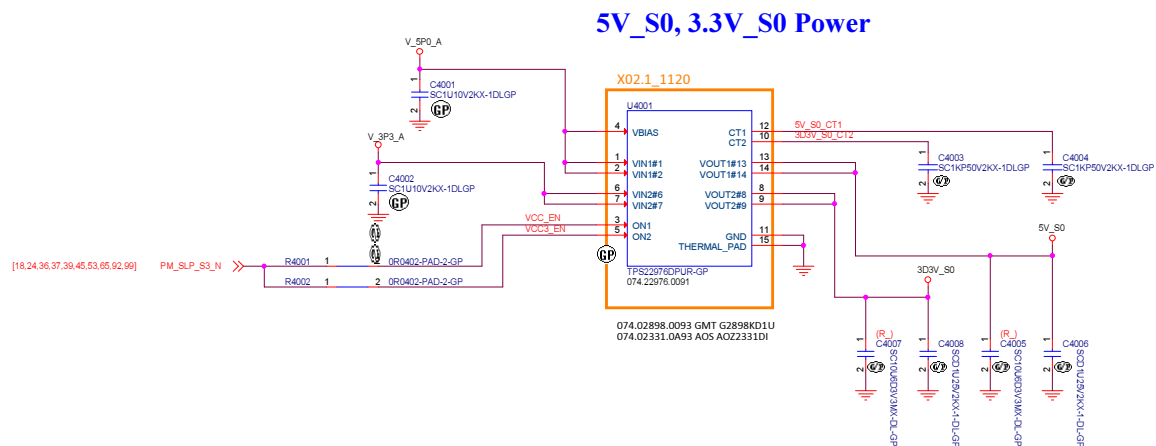
ODMs need to work with Cypress to Get the CCG4_ID_2 Assigned for the Platform. Cypress will be maintaining the P

Group	Sub Group	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1		Single Port – DFP with USB Only	L0	Lx
2		Single Port – DFP + DP Alt Mode	L2	Lx
3		Dual Port – DFP with USB Only on Both Ports	L3	Lx
	a	Configuration 32 – DFP + USB Only in both ports	L3	L7
4		Dual Port – DFP + DP on Port 1 , DFP with USB only on Port 2	L4	Lx
5		Dual Port – DFP + DP on Both Ports	L6	Lx
	a	Configuration 56 – DFP + DP on both Ports	L6	L7

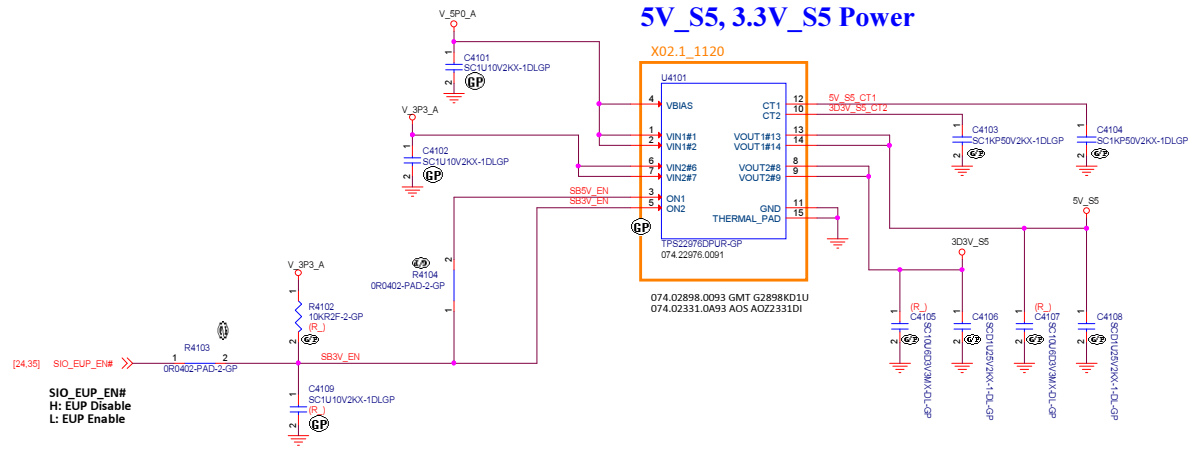
Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8



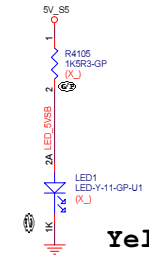
3D3V_S0 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,45,53,54,55,56,57,58,59,61,62,63,64,65,66]
V_3P3_A V_3P3_A [24,25,41,44,64]
5V_S0 5V_S0 [24,26,27,54,55,57,64,65,66,92,94]
V_5P0_A V_5P0_A [27,28,34,35,36,37,39,41,44,45,46,48,89,92]



3D3V_S5 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,38,42,45,61,63,65,95,96,99]
V_3P3_A V_3P3_A [24,25,40,44,64]
5V_S5 5V_S5 [30,42,63,64,95,96]
V_5P0_A V_5P0_A [27,28,34,35,36,37,39,40,44,45,46,48,89,92]



5V_S5 LED

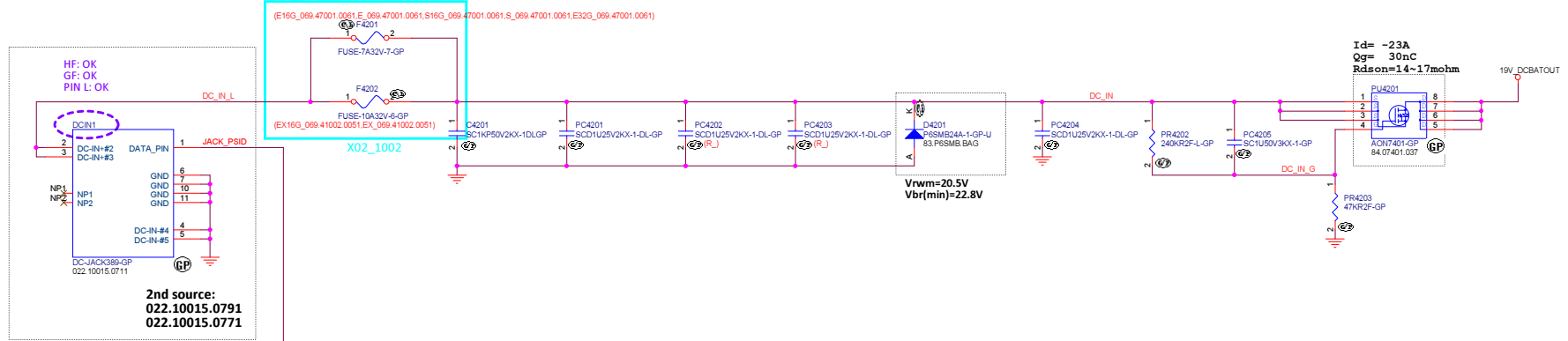


Yellow LED

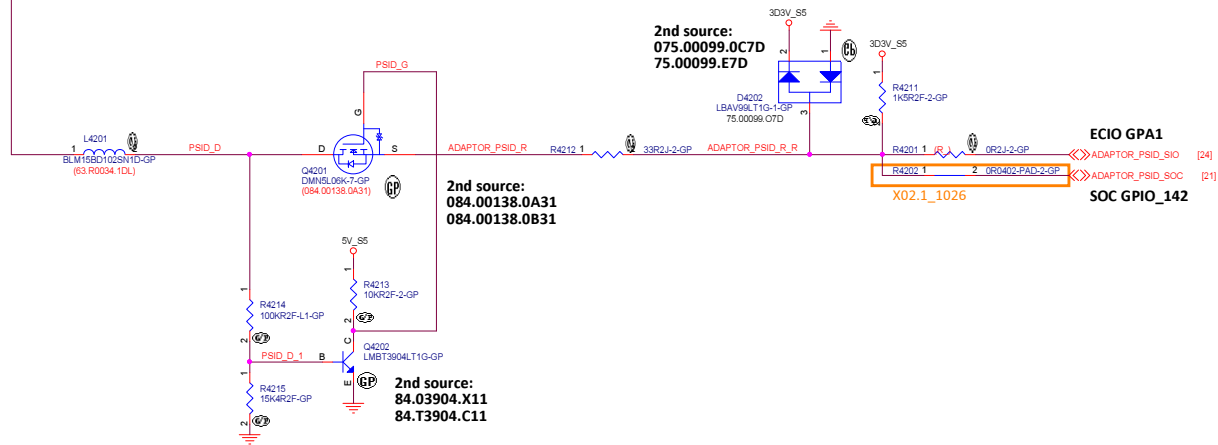
SIO_EUP_EN#
H: EUP Disable
L: EUP Enable

19V_DCBATOUT 19V_DCBATOUT [44,45,46,48,65,69]
 3D3V_S5 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,39,41,45,61,63,65,66,96,99]
 5V_S5 5V_S5 [30,41,63,64,96,99]

7A for 65W/90W
 10A for 130W

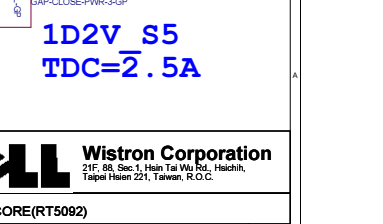
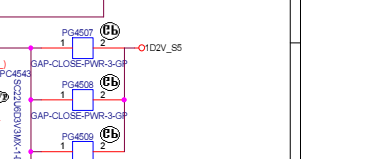
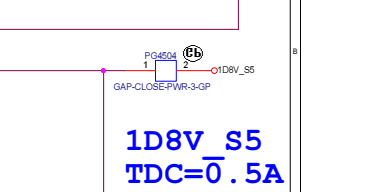
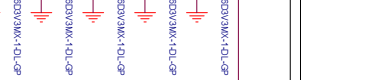
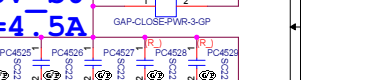
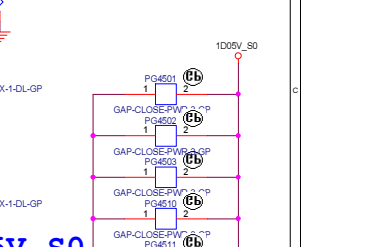
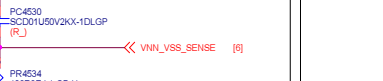
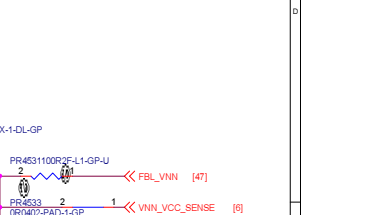
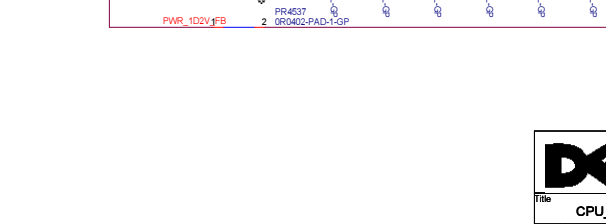
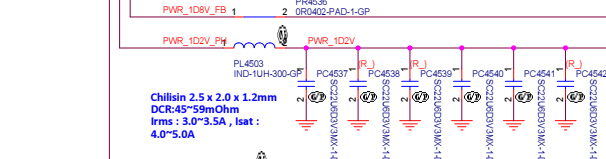
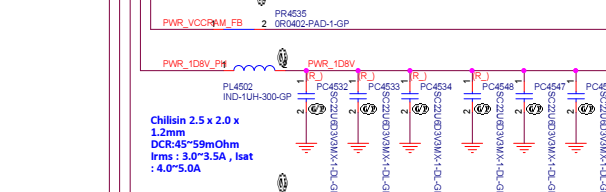
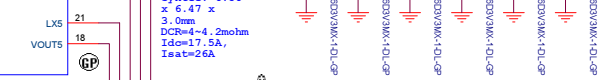
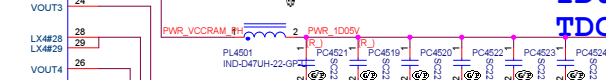
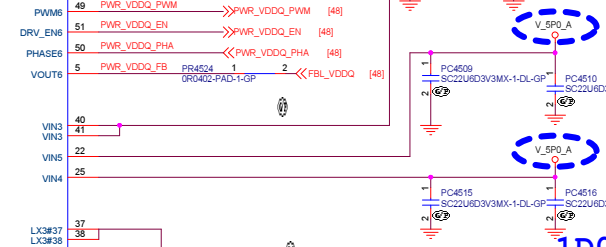
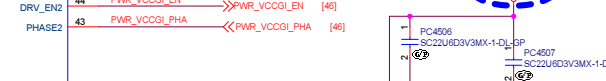
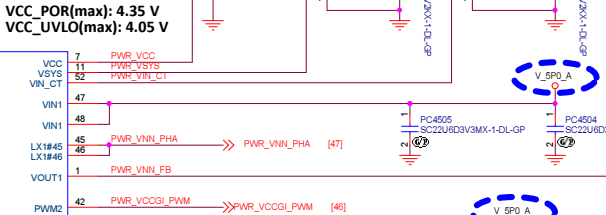
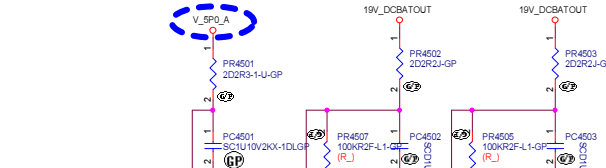
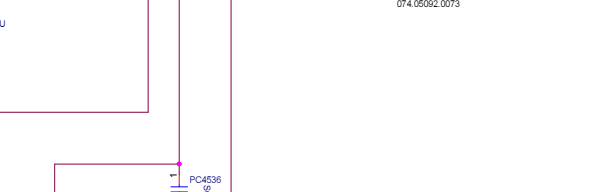
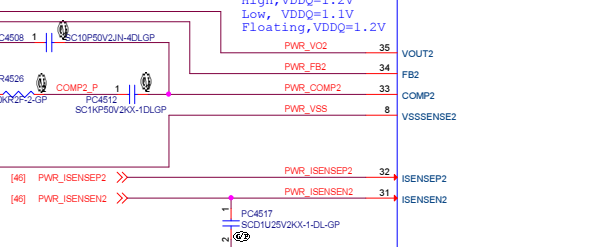
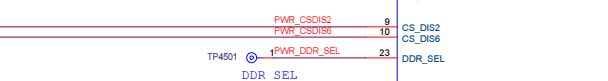
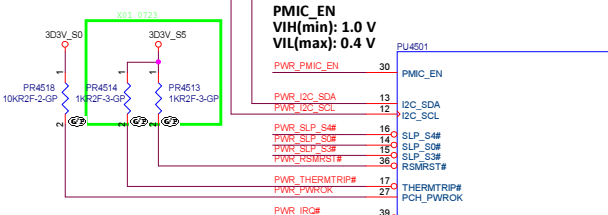
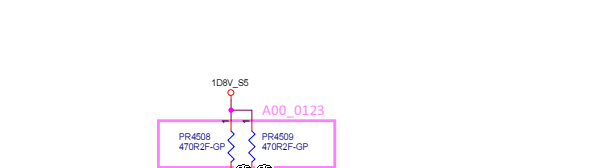
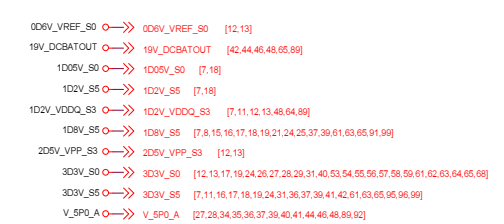
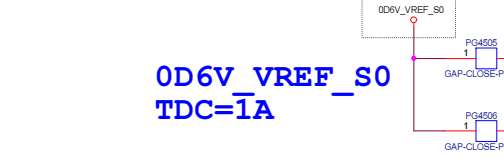
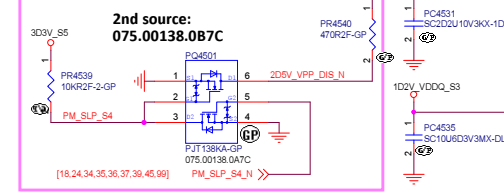
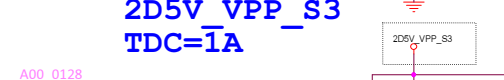
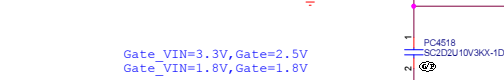
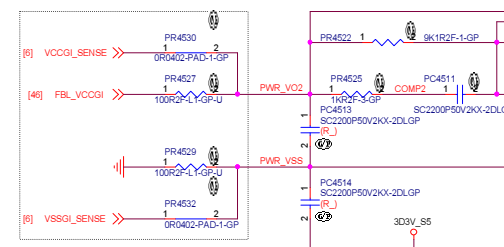
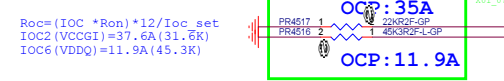
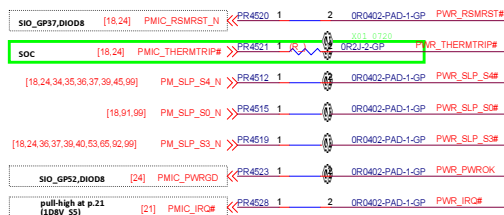
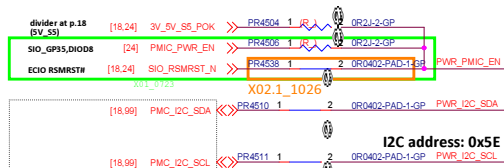


PSID (Follow Dell EEIG)

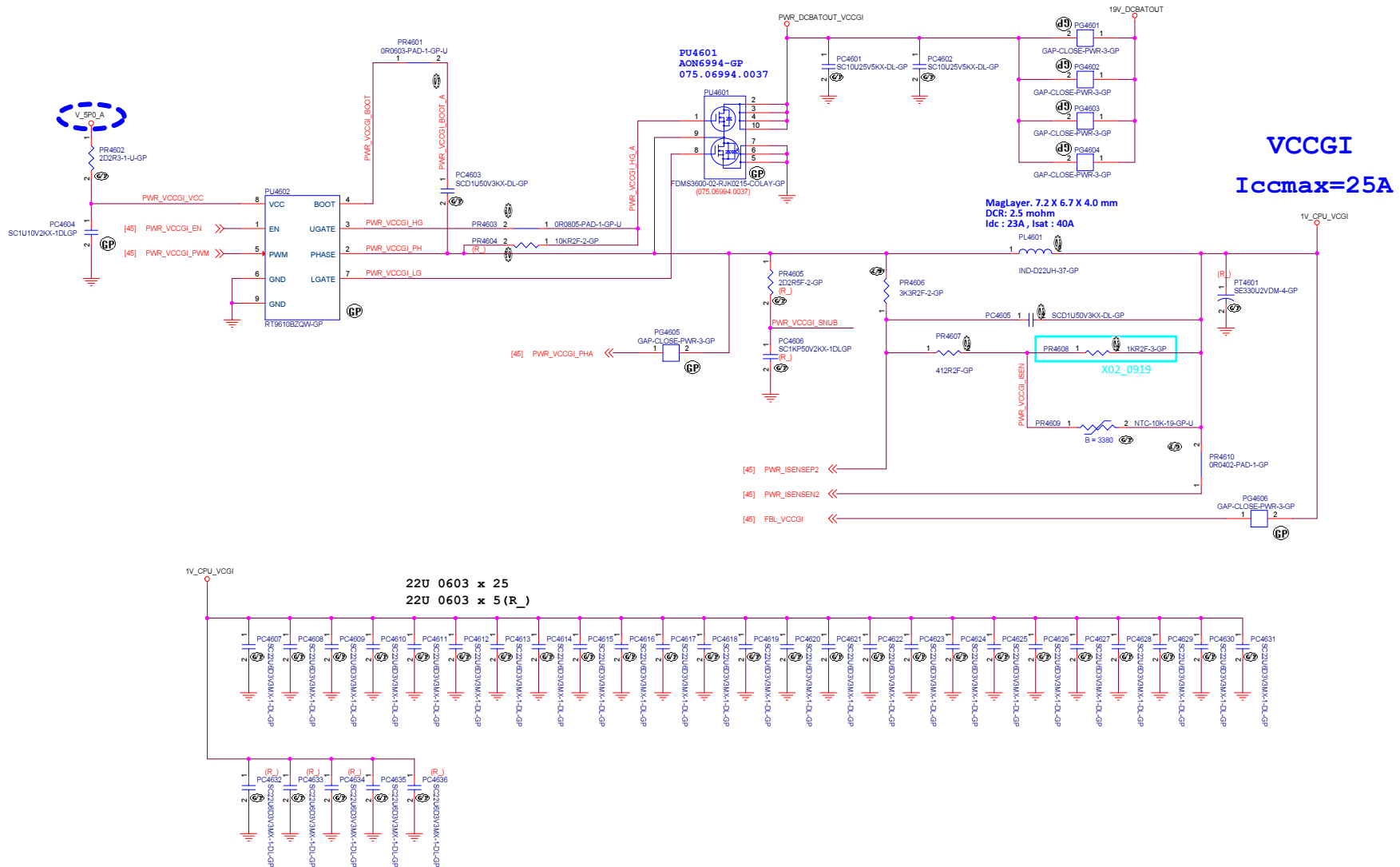


PWR_12V

Blanking



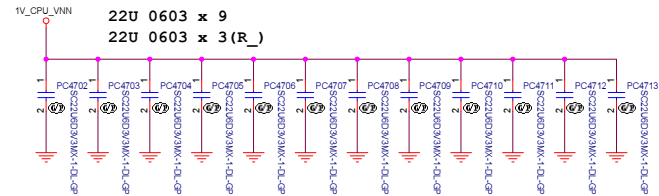
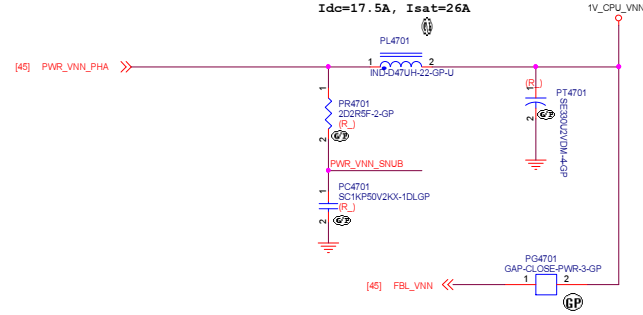
19V_DCBATOUT → 19V_DCBATOUT [42,44,45,48,65,89]
 1V_CPU_VCGI → 1V_CPU_VCGI [8,10,64]
 V_SP0_A → V_SP0_A [27,28,34,35,36,37,39,40,41,44,45,48,89,92]



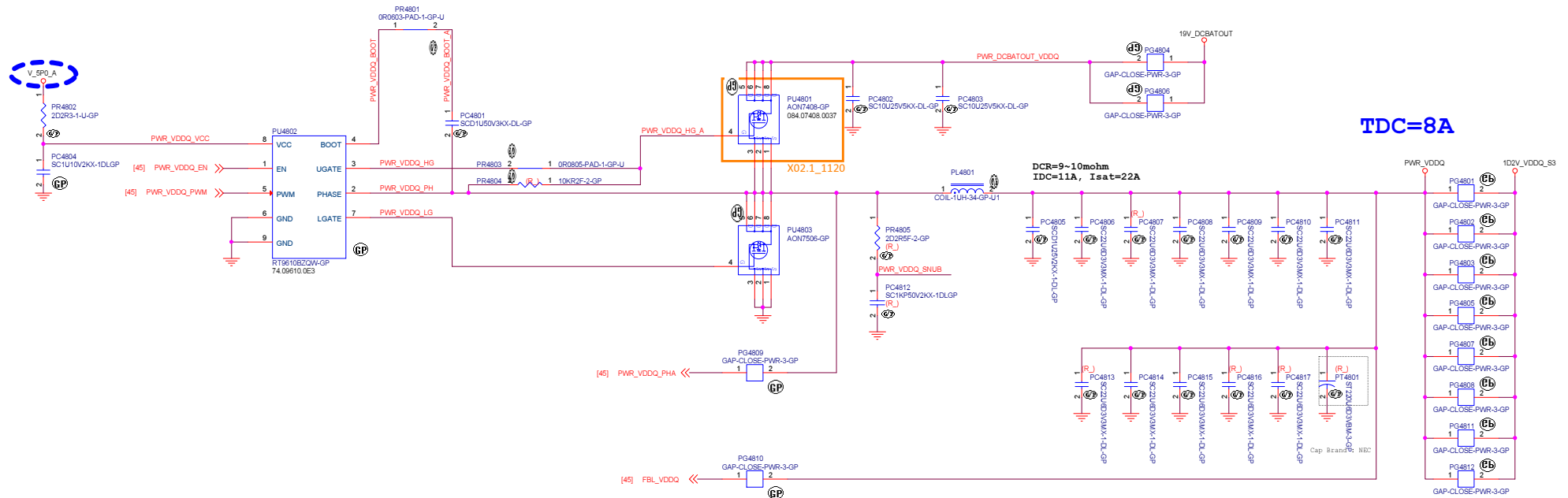
1V_CPU_VNN 0--> 1V_CPU_VNN [6,10,89]

VNN Iccmax=4A

Cyntec. 6.86 x 6.47 x 3.0mm
DCR=4~4.2mohm
Idc=17.5A, Isat=26A



19V_DCBATOUT ○→ 19V_DCBATOUT [42,44,45,46,65,69]
 1D2V_VDDQ_S3 ○→ 1D2V_VDDQ_S3 [7,11,12,13,45,64,69]
 V_5P0_A ○→ V_5P0_A [27,28,34,35,36,37,39,40,41,44,45,46,69,92]



TDC=8A

Blanking

Blanking

Blanking

Blanking

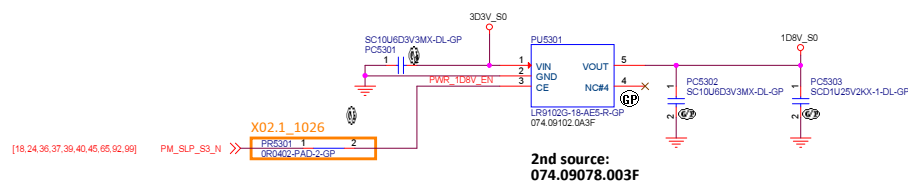
3D3V_S0 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,54,55,56,57,58,59,61,62,63,64,65,68]

1.8V S0

Imax = 300mA

Design Note:

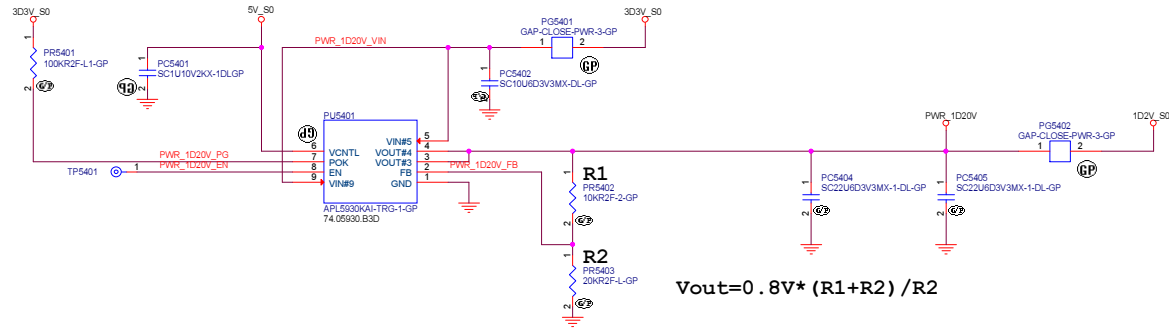
Design Note:
NPCT750 for TPM -- 5mA
64GB for eMMC -- 230mA
ALC3253 for Codec -- 5mA



2nd source:
074.09078.003F

5V_S0 → 5V_S0 [24,26,27,40,56,57,64,65,66,92,94]
 3D3V_S0 → 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,55,56,57,58,59,61,62,63,64,65,68]
 1D2V_S0 → 1D2V_S0 [55,58,59,64]

1D2V_S0 for PS181/PS8468



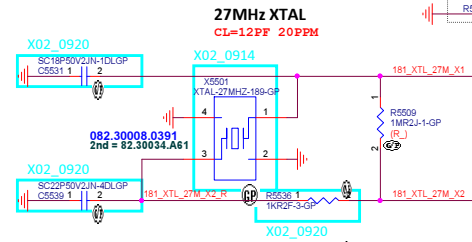
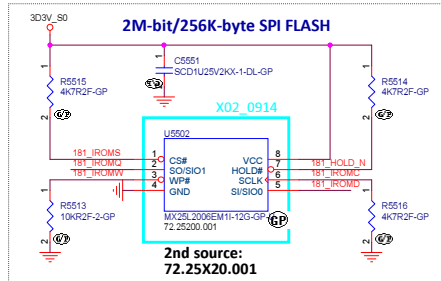
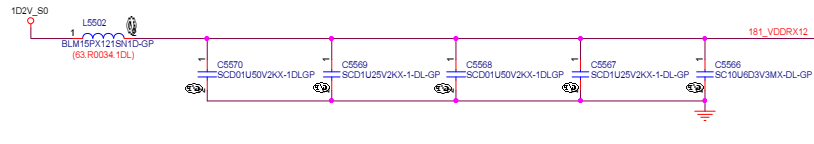
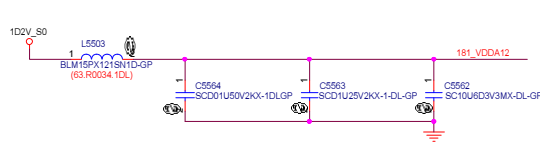
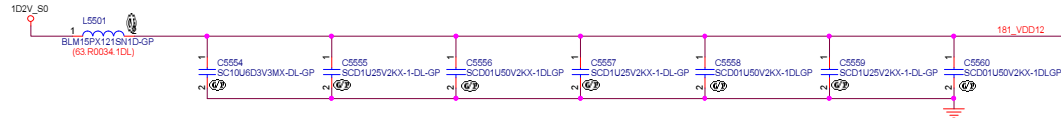
1D2V

IDC = 1400mA
 Imax = 3000mA

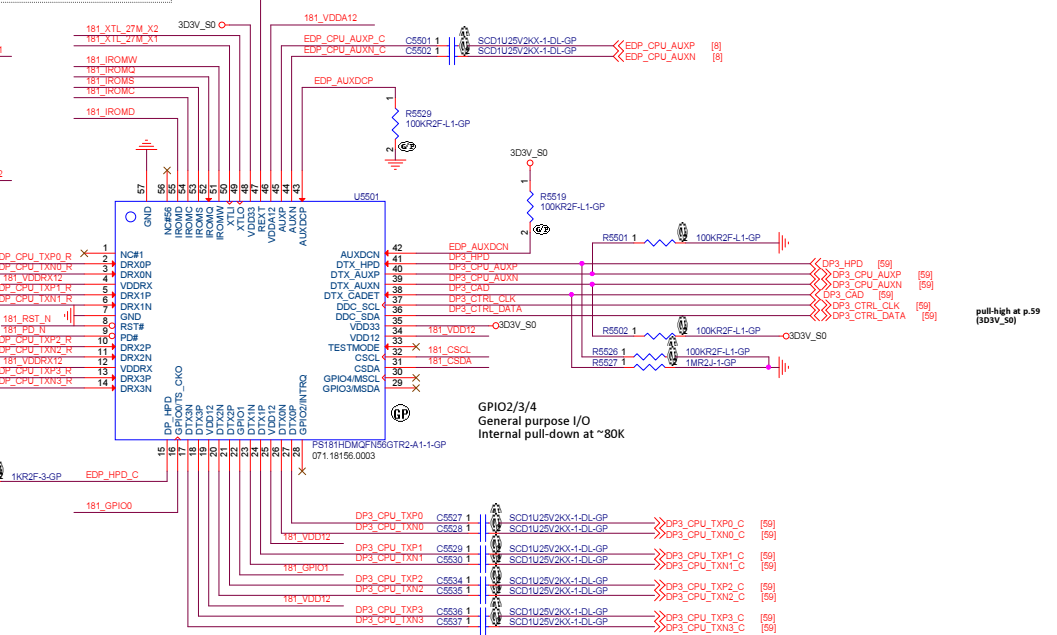
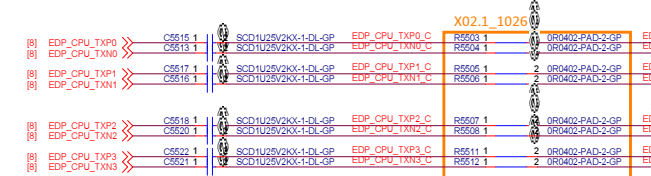
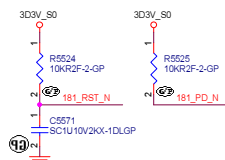
Design Note:
 PS181 -- 492mA
 PS8468 for DP2 -- 450mA
 PS8468 for DP3 -- 450mA

303V_S0 → 303V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,56,57,58,59,61,62,63,64,65,68]

102V_S0 → 102V_S0 [54,58,59,64]



4K99 ohm should be placed close to PS181 REXT pin
Add ground shielding between REXT and XTLO/XTLI



Power On Configuration

303V_S0 → R5530 1 4K7R2F-GP (R) 181_IROMD

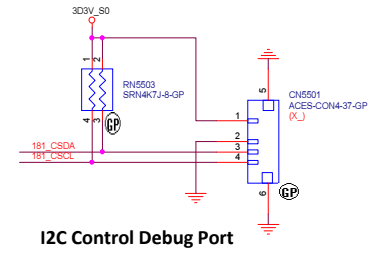
IROMD: Firmware Initial Address, internal pull-down ~80K
0: Start from Bank 3
1: Start from Bank 7

303V_S0 → R5523 1 4K7R2F-GP (R) 181_GPIO0

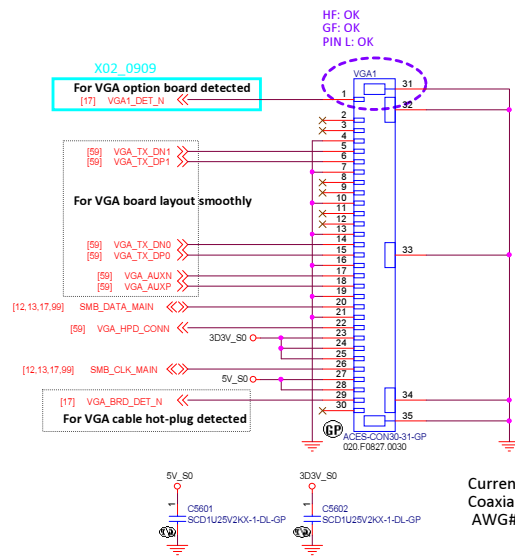
GPIO0: Control I2C address selection, internal pull-down ~80K
0: 0x10h - 0x2Fh (default)
1: 0x90h - 0x9Fh, 0xD0h - 0xDFh

303V_S0 → R5531 1 4K7R2F-GP (R) 181_GPIO1

GPIO1: MPU/I2C select, internal pull-down ~80K
0: Use MPU to control PS181 (default)
1: Use control I2C to control PS181



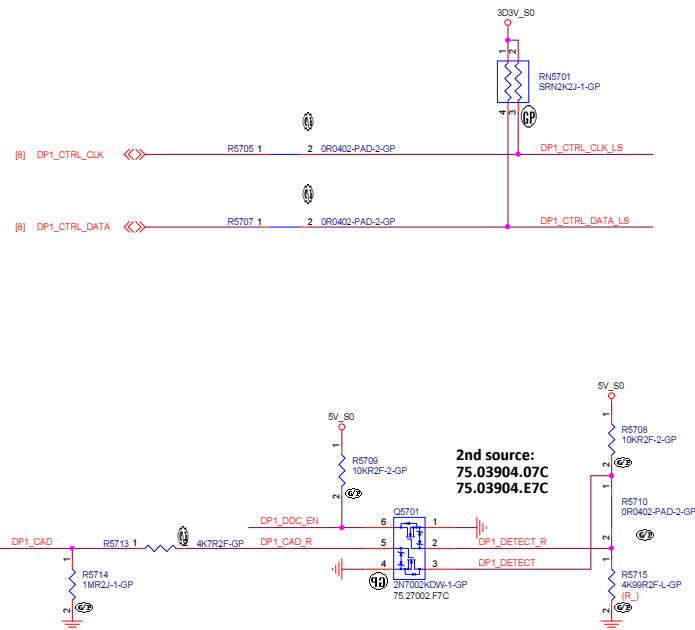
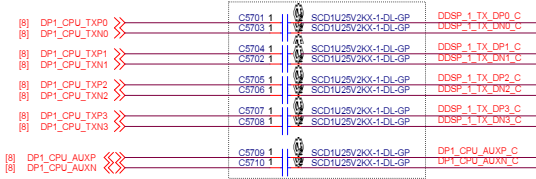
3D3V_S0 ○ → 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,57,58,59,61,62,63,64,65,68]
5V_S0 ○ → 5V_S0 [24,26,27,40,54,57,64,65,66,92,94]



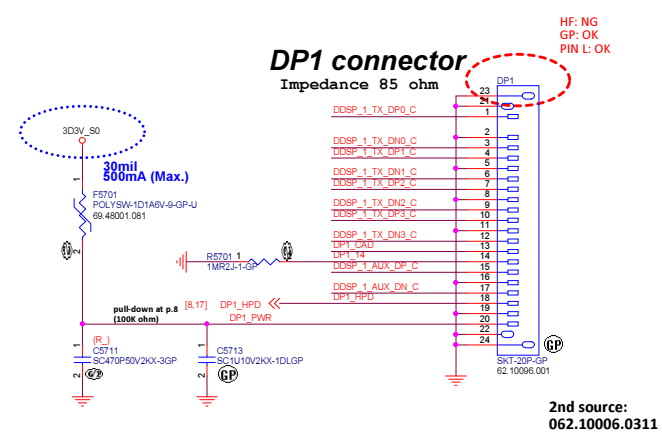
Current: 0.3~0.2 Amperes /pin (depending on the diameter of cable conductor)
Coaxial cables:
AWG#36: 0.30A AC,DC PER CONTACT

2nd source:
020.K0218.0030

Place all CAPs near DP Connector



DESIGN NOTE:
WHEN HDMI CONNECTED: CONFIG1 - HIGH,
WHEN DP CONNECTED: CONFIG1 - LOW



The diagram shows the timing of DP1 signals. The signals are grouped into three sections, each with a 7505 or 7506 comparator and a 7504 multiplexer. The signals are: DSDSP_1_AUX_DN_C, DP1_HP_D, DP1_CAD, DSDSP_1_TX_DP2_C, DSDSP_1_TX_DN2_C, DSDSP_1_TX_DP3_C, DSDSP_1_TX_DN3_C, DSDSP_1_TX_DP0_C, DSDSP_1_TX_DN0_C, DSDSP_1_TX_DP1_C, and DSDSP_1_TX_DN1_C. The comparators are labeled 7505 and 7506, and the multiplexer is labeled 7504. The power supply is L06ESD5LV0NA-4-GP (075.00550.0071 (R_)).

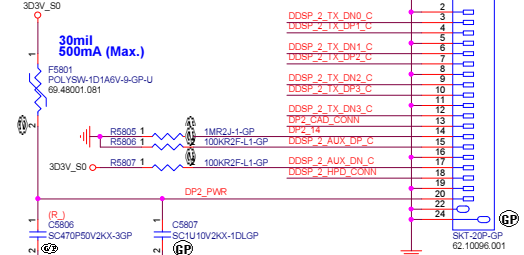
2nd source:
75.08808.073
075.01043.0073



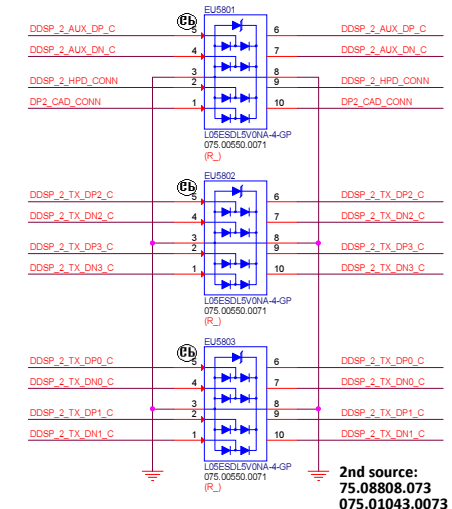
CFG1
Automatic EQ configuration;
internal pull down at 150K ohm, 3.3V I/O
L: Auto EQ enabled, EQ automatically adjusted based on link training.
H: Auto EQ disabled.

Impedance 85 ohm

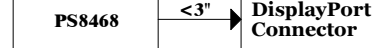
I2C_ADDR
I2C control enable and address.
Internally pulled down at ~150K ohm, 3.3V I/O
L: Default I2C address, 0x10-0x2F
H: Alternative I2C address, 0x90-0x9F; 0xD0-0xDF



ESD Diodes




2nd source:
75.08808.073
075.01043.0073



DESIGN NOTE:
WHEN HDMI CONNECTED: DP_CA_DET_x - HIGH,
WHEN DP CONNECTED: DP_CA_DET_x - LOW

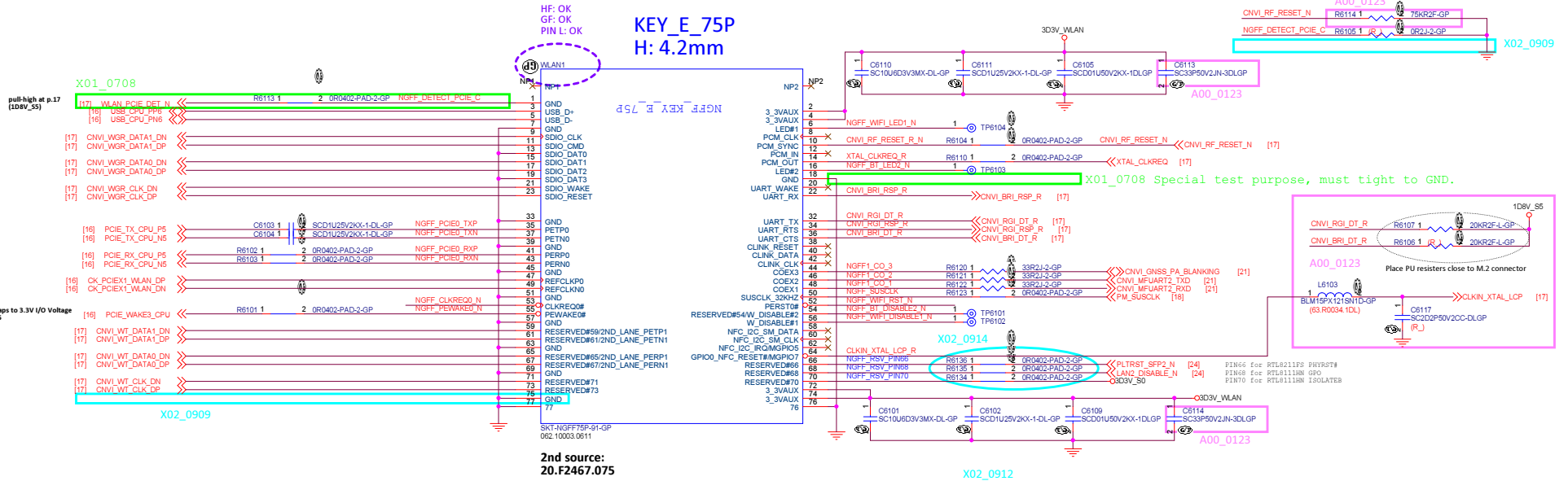


Blanking

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size C	Document Number San Bernardino		Rev N00
Date: Thursday, March 08, 2018		Sheet 60 of	106

NGFF(Hybrid Key-E for DISCRETE/CNVI)

1D8V_S5 → 1D8V_S5 [7,8,15,16,17,18,19,21,24,25,37,39,45,63,65,91,99]
 3D3V_S5 → 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,39,41,42,45,63,65,95,96,99]
 3D3V_S0 → 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,62,63,64,65,68]



3D3V_S0 → 3D3V_S0 [12, 13, 17, 19, 24, 26, 27, 28, 31, 40, 45, 53, 54, 55, 56, 57, 58, 59, 61, 63, 64, 65, 66]

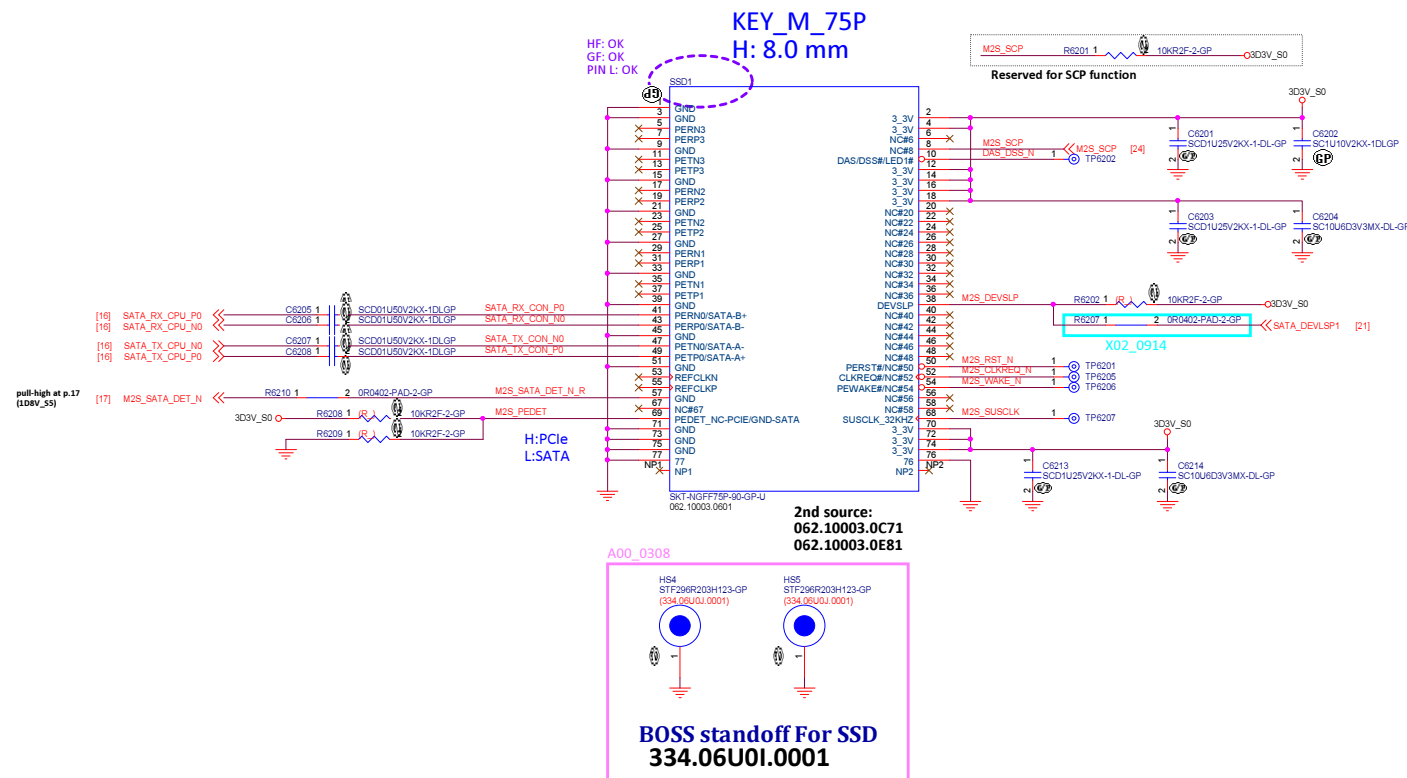
Table 47. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - SATA	N/A
0	0	1	0	WWAN - PCIe	0
0	1	1	0	WWAN - PCIe	1

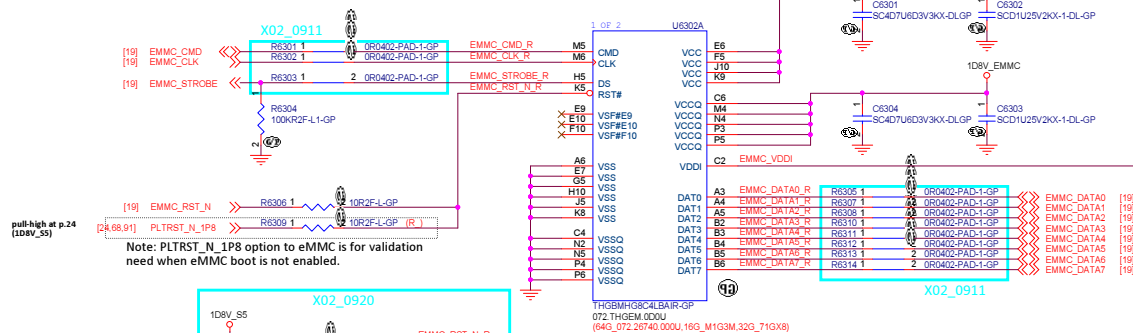
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

34	2.5V	GND	75
72	2.5V	GND	73
70	2.5V	GND	71
68	SUSCLK(32kHz) (IO)(0V/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PERWAKE(U/I)(0V/3.3V) or N/C	REFCLKN	53
52	CURREQ(U/I)(0V/3.3V) or N/C	GND	51
50	PERST#(O/I)(0V/3.3V) or N/C	PET3(SATA-A+)	49
48	N/C	PET3(SATA-A-)	47
46	N/C	GND	45
44	N/C	PER0(SATA-B-)	43
42	N/C	PER0(SATA-B+)	41
40	N/C	GND	39
38	DEVSUP (D)	PET1	37
36	N/C	PET1	35
34	N/C	GND	33
32	N/C	PER1	31
30	N/C	PER1	29
28	N/C	GND	27
26	N/C	PET2	25
24	N/C	PET2	23
22	N/C	GND	21
20	N/C	PER2	19
18	2.5V	PER2	17
16	2.5V	GND	15
14	2.5V	PET3	13
12	2.5V	PET3	11
10	DAS/DSS#(U/I)(0V/3.3V)	GND	9
8	N/C	PER3	7
6	N/C	PER3	5
4	2.5V	GND	3
2	2.5V	GND	1

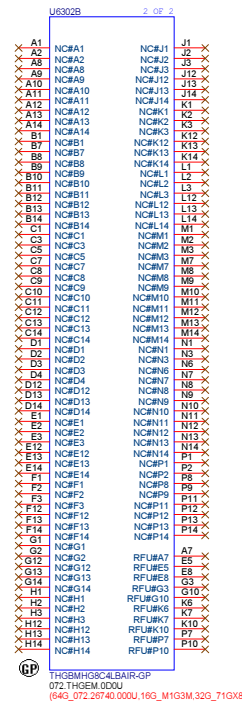
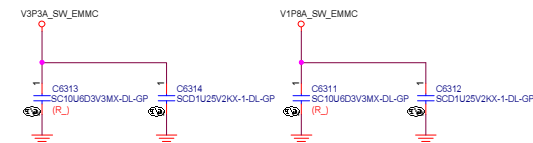
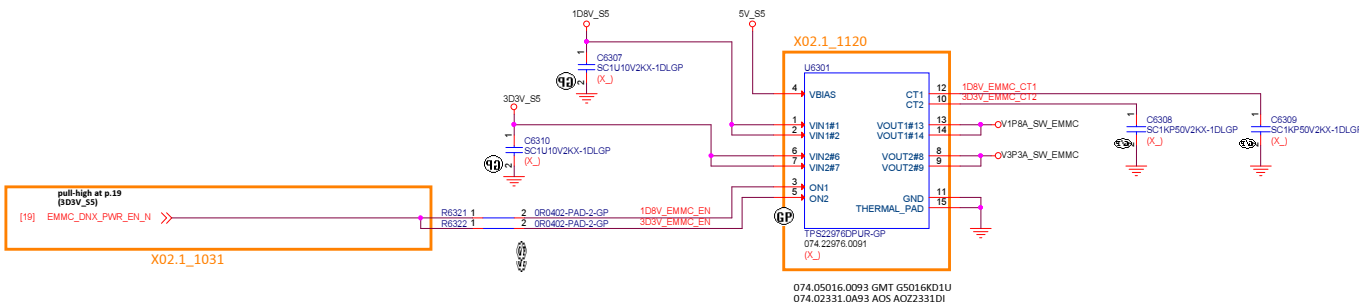
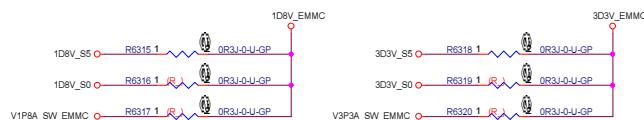
M.2 2260/2280 Key M Type (SATA Only)



1D8V_S0 → 1D8V_S0 [27,53,64,91]
 1D8V_S5 → 1D8V_S5 [7,8,15,16,17,18,19,21,24,25,37,39,45,61,65,91,99]
 3D3V_S0 → 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,64,65,68]
 3D3V_S5 → 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,39,41,42,45,61,65,95,96,99]
 5V_S5 → 5V_S5 [39,41,42,64,95,99]

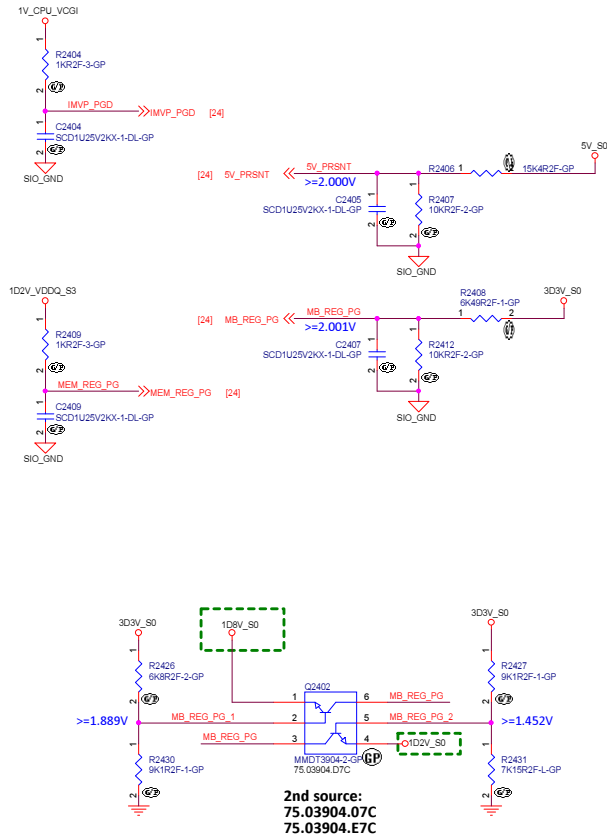


Note:
 (64G_164G: 072.26740.000U(H26M74002EMR)
 (16G_116G: M1G3M (Hynix), G82Y4 (SanDisk)
 (32G_32G: 71GX8 (Hynix), HC8MM (SanDisk)

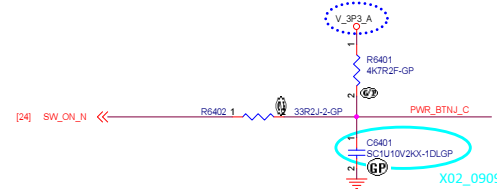


1D8V_S5 O → 1D8V_S5 [7,8,15,16,17,18,19,21,24,25,37,39,45,61,63,65,91,99]
 3D3V_S0 O → 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,65,68]
 5V_S0 O → 5V_S0 [24,26,27,40,54,56,57,66,62,94]
 5V_S5 O → 5V_S5 [39,41,42,63,95,96]
 V_3P3_A O → V_3P3_A [24,25,40,41,44]
 1D8V_S0 O → 1D8V_S0 [27,53,63,91]
 1D2V_S0 O → 1D2V_S0 [54,55,58,59]
 1D2V_VDDQ_S3 O → 1D2V_VDDQ_S3 [7,11,12,13,45,48,89]
 1V_CPU_VCGI O → 1V_CPU_VCGI [6,10,46]
 2D5V_VPP_S3 O → 2D5V_VPP_S3 [12,13,45]
 1D05V_S0 O → 1D05V_S0 [7,18,45]

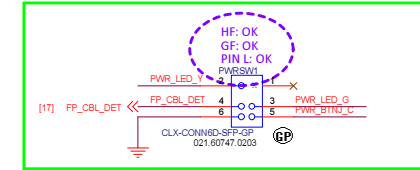
Circuit to Support pre-Post Diagnostic



POWER BUTTON with PWR/SUS LED

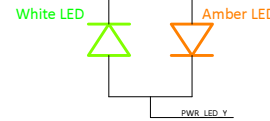


X01_0708



2nd source:
021.60966.0203

POWER LED



Dual color, white/amber

Off: system off

During POST:

Solid Amber: system booting in progress or fault, power ok

Blinking Amber: power is bad

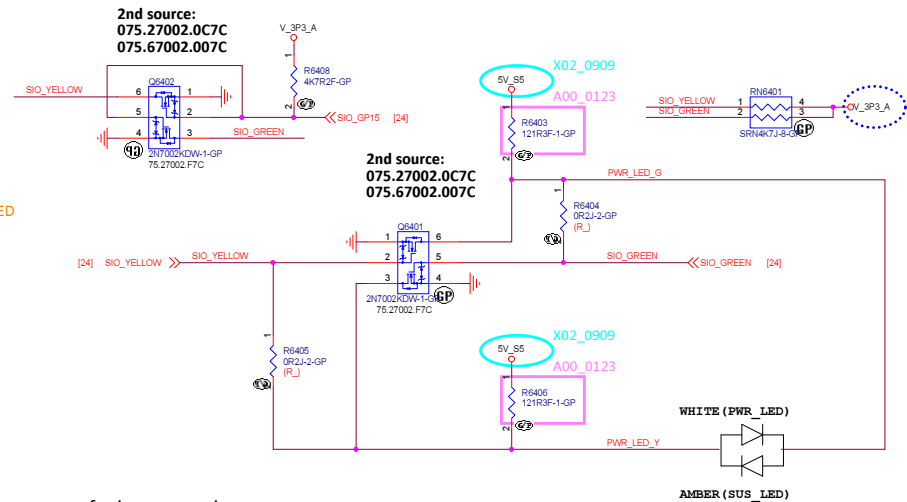
S3 (sleep) state: Breathing White

Dark to bright 2.5s - gradually dimming

Bright to dark 2.5s - gradually dimming

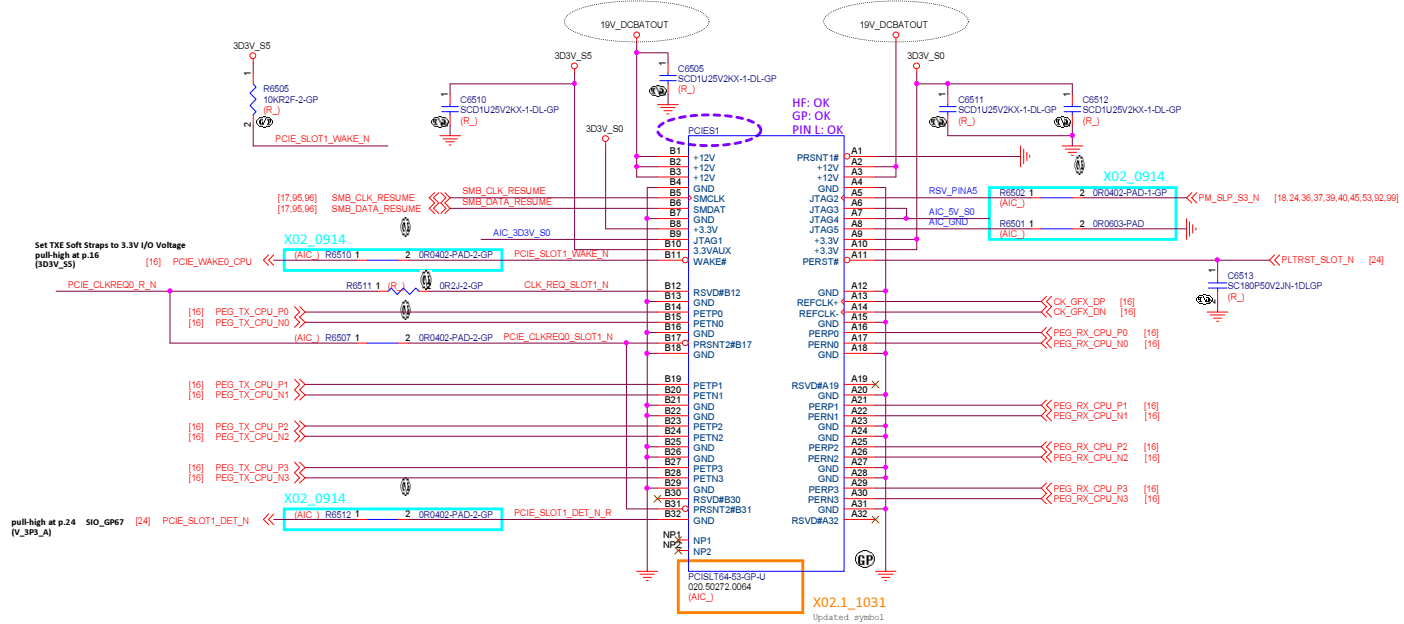
S0 (on) state: Solid White

See desktop behavior spec for more details

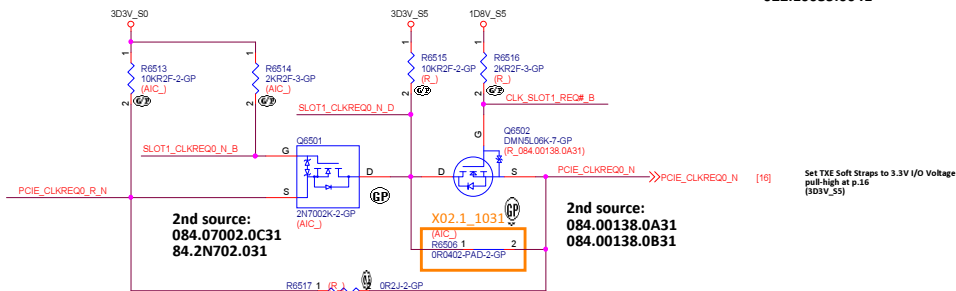
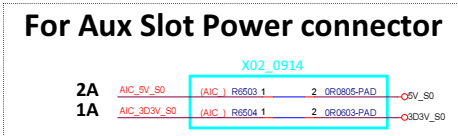


	SIO_YELLOW	SIO_GREEN
AMBER(SUS_LED)	L	H
WHITE(PWR_LED)	H	L

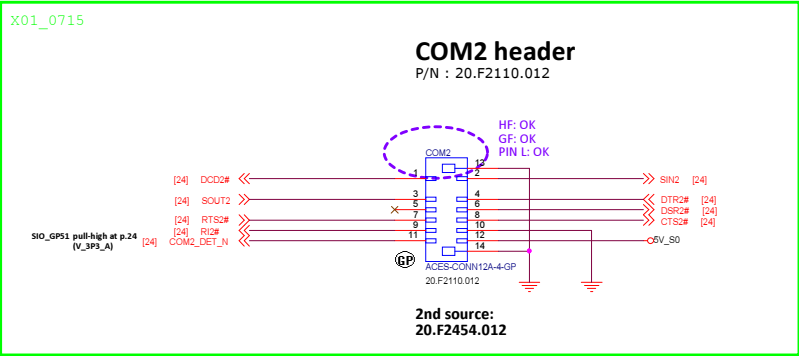
1D8V_S5 <--> 1D8V_S5 [7,8,15,16,17,18,19,21,24,25,37,39,45,61,63,91,99]
 3D3V_S0 <--> 3D3V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,68]
 3D3V_S5 <--> 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,39,41,42,45,61,63,95,96,99]
 5V_S0 <--> 5V_S0 [24,26,27,40,54,56,57,64,66,92,94]
 19V_DCBATOUT <--> 19V_DCBATOUT [42,44,45,46,48,89]



2nd source:
022.10035.0041



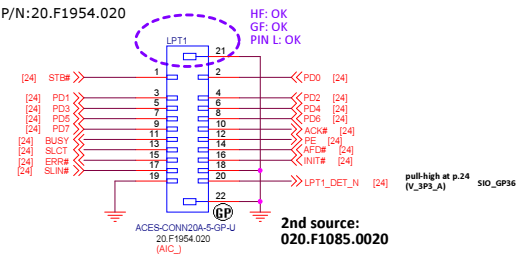
5V_S0 5V_S0 [24,26,27,40,54,56,57,64,65,92,94]



ACES 50238 series
Working voltage less than 36 volts (per pin)
Voltage: 50 Volts AC (per pin)
Current: 1 Amperes (per pin)

LPT header

P/N:20.F1954.020



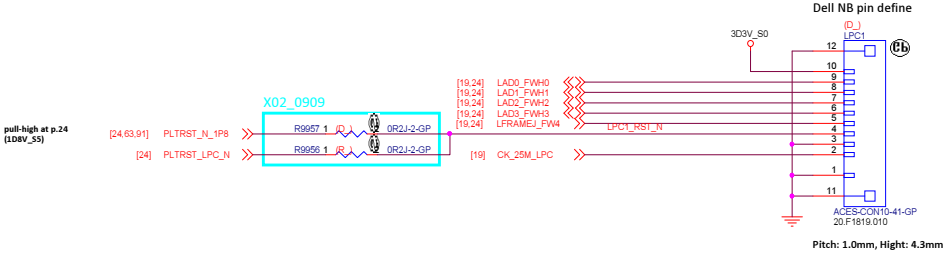
ACES 50238; 50425 series
Working voltage less than 36 volts (per pin)
Voltage: 50 Volts AC (per pin)
Current: 1 Amperes (per pin)

X01_0715.

Blanking

3D8V_S0 o-->> 3D8V_S0 [12,13,17,19,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65]


PORT 80 Connector
Debug only



Blanking


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taippei Hsien 221, Taiwan, R.O.C.
Title (Reserved)		
Size C	Document Number San Bernardino	Rev N00
Date: Thursday, March 08, 2018		Sheet 69 of 106

Blanking

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size C	Document Number San Bernardino		Rev N00
Date: Thursday, March 08, 2018		Sheet 70 of	106

Blanking

Blanking

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size C	Document Number San Bernardino		Rev N00
Date: Thursday, March 08, 2018		Sheet 72 of	106

Blanking

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size C	Document Number San Bernardino		Rev N00
Date: Thursday, March 08, 2018		Sheet 73 of	106

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

Blanking

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Haichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
(Reserved)			
Size	Document Number		Rev
C	San Bernardino		N00
Date: Thursday, March 08, 2018		Sheet 88 of	106

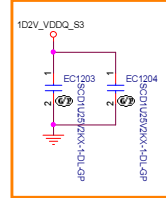
1V_CPU_VNN → 1V_CPU_VNN [6,10,47]
102V_VDDQ_S3 → 102V_VDDQ_S3 [7,11,12,13,45,48,64]
V_SP0_A → V_SP0_A [27,28,34,35,36,37,39,40,41,44,45,46,48,52]

19V_DCBATOUT → 19V_DCBATOUT [42,44,45,46,48,65]
AGND → AGND [26,27,28,29]

Stitching Capacitors

DIMM1

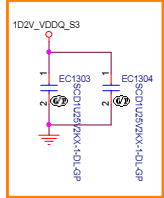
For stitching capacitor



0.1uF*2

DIMM2

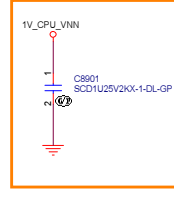
For stitching capacitor



0.1uF*2

BSSB_CLK

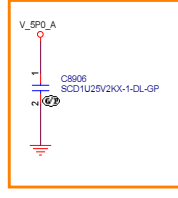
For stitching capacitor



0.1uF*1

GP_SSP0_FS1

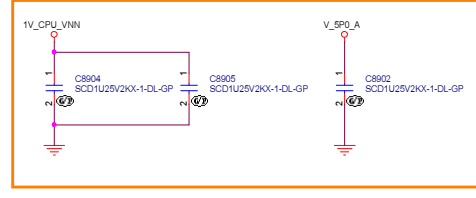
For stitching capacitor



0.1uF*1

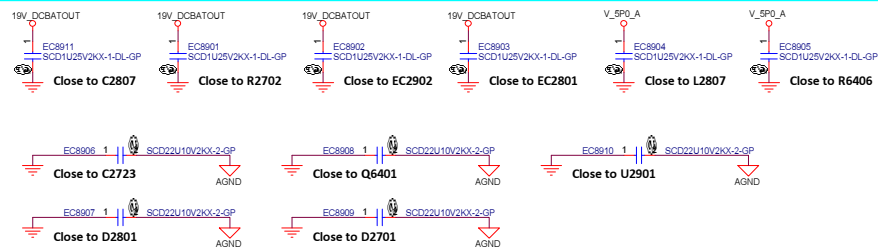
PMIC_PWR_EN

For stitching capacitor



0.1uF*2

X02_0915



Blanking

1D8V_S5 → 1D8V_S5 [7, 8, 15, 16, 17, 18, 19, 21, 24, 25, 37, 39, 45, 61, 63, 65, 99]

3D3V_S5 → 3D3V_S5 [7, 11, 16, 17, 18, 19, 24, 31, 36, 37, 39, 41, 42, 45, 61, 63, 65, 95, 96, 99]

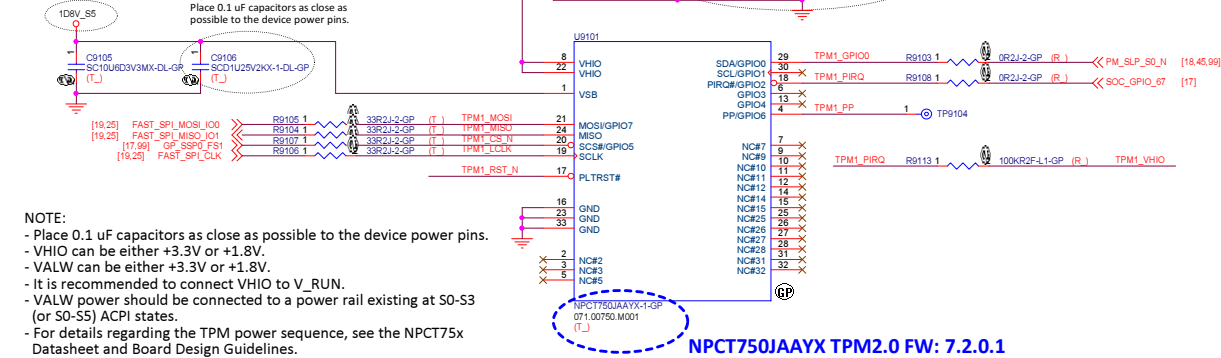
1D8V_S0 → 1D8V_S0 [27, 53, 63, 64]

Nuvoton TPM

X01_0722

Vendor recommend

NOTE:
Place 0.1 uF capacitors as close as possible to the device power pins.



NOTE:

- Place 0.1 uF capacitors as close as possible to the device power pins.
- V_HIO can be either +3.3V or +1.8V.
- VALW can be either +3.3V or +1.8V.
- It is recommended to connect V_HIO to V_RUN.
- VALW power should be connected to a power rail existing at S0-S3 (or S0-S5) ACPI states.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

X02_0821

Removed level shift circuit

pull-high at p.24
(1D8V_S5)

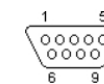
[24, 63, 68] PLTRST_N_1P8

X02_1_1026

5V_S0 → 5V_S0 [24,26,27,40,54,56,57,64,65,66,94]
V_SPO_A → V_SPO_A [27,28,34,35,36,37,39,40,41,44,45,46,48,89]

COM1

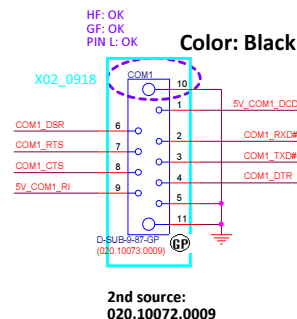
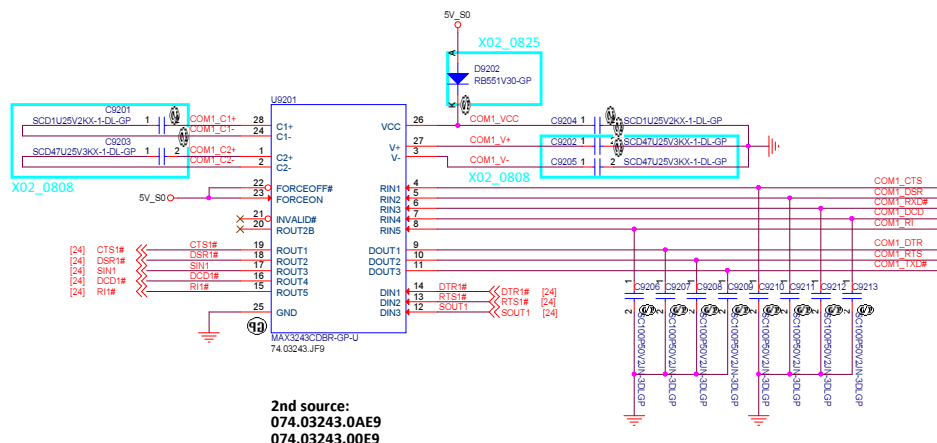
Vcc	C9201	C9202,C9203 and C9205
3.3V±0.3V	0.1uF	0.1uF
5V±0.5V	0.047uF	0.33uF
3V to 5.5V	0.1uF	0.47uF



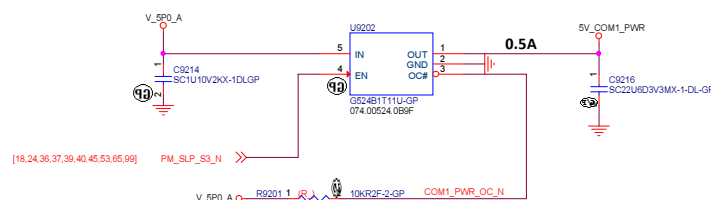
9 pin DE9 male connector at the computer.



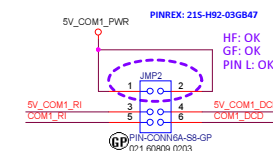
10 pin IDC male connector at motherboard.



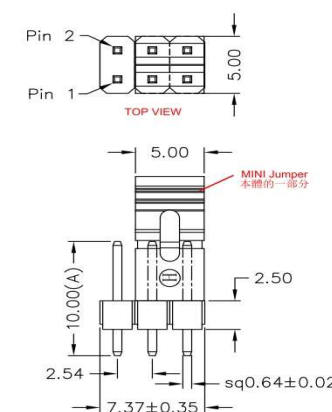
DE9 Pin	IDC 10 Pin	Name	Dir	Description
1	1	CD	IN	Carrier Detect
2	3	RXD	IN	Receive Data
3	5	TXD	OUT	Transmit Data
4	7	DTR	OUT	Data Terminal Ready
5	9	GND	-	System Ground
6	2	DSR	IN	Data Set Ready
7	4	RTS	OUT	Request to Send
8	6	CTS	IN	Clear to Send
9	8	RI	IN	Ring Indicator



Jumper	Function	Label	Operation
JMP2	RI switch to 5V	RI to 5V	1 - 3 Short : 5V
	DCD switch to 5V	DCD to 5V	2 - 4 Short : 5V
	RI signal	RI	3 - 5 Short : RI (Default)
	DCD signal	DCD	4 - 6 Short : DCD (Default)



Mini jumper setting
(1-3,2-4) for 5V
(3-5,4-6) for RI,DCD --> Default



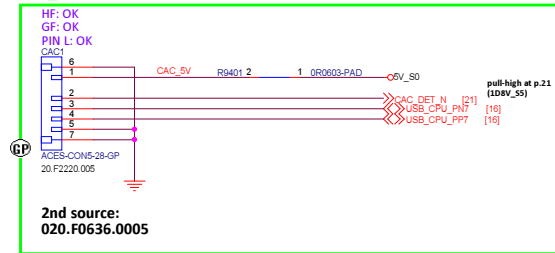
Blanking

5V_S0 >> 5V_S0 [24,26,27,40,54,56,57,64,65,66,92]

New part: 50228-00571-001
Change from 8 pin to 5 pin

Current:
AWG#28: 1.0 A, (per pin)

X01_0715



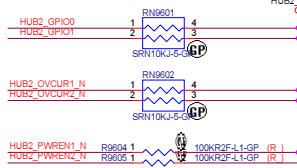
3D3V_S5 << 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,30,41,42,45,61,63,65,95,96]
5V_S5 >> 5V_S5 [36,41,42,63,64,95]

SPWR_DET
0: Bus-power setting
1: Self-power setting

BPWR_DET
0: Upstream VBUS Power is absent
1: Upstream VBUS Power exists

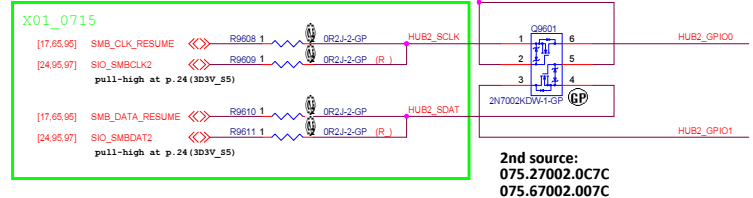
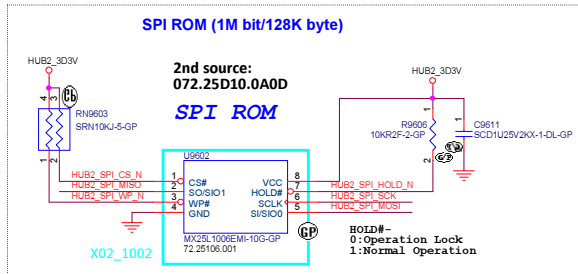
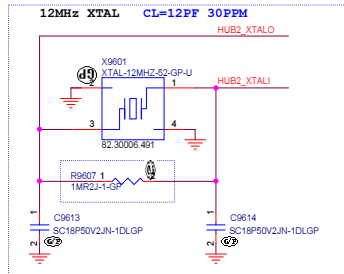
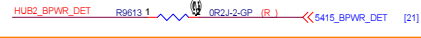
Vendor recommend

X02_0824

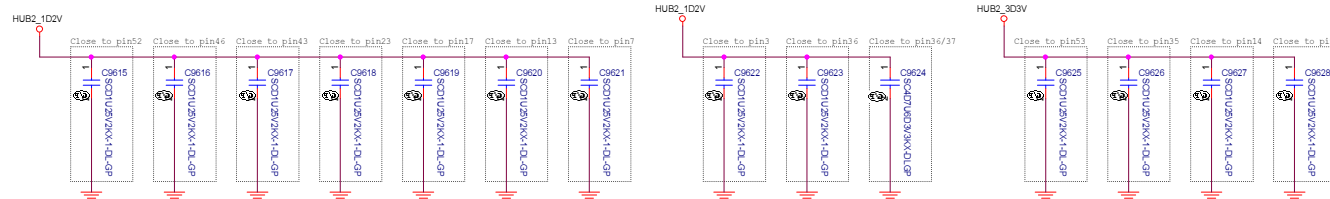


Note:
The GPIO0 can be configured as a SMBus clock pin
The GPIO1 can be configured as a SMBus data pin
The GPIO2 can be configured as an I2C clock pin
The GPIO3 can be configured as an I2C data pin

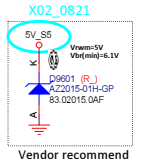
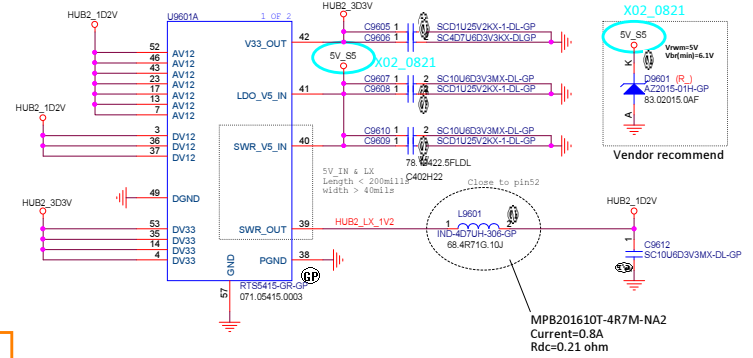
X02_1_1113



2nd source:
075.27002.0C7C
075.67002.007C



From SOC USB2 port 5
From SOC USB3 port 5
To SOC USB3 port 5



MPB201610T-4R7M-NA2
Current=0.8A
Rdc=0.21 ohm



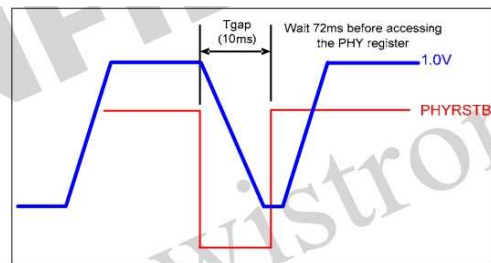
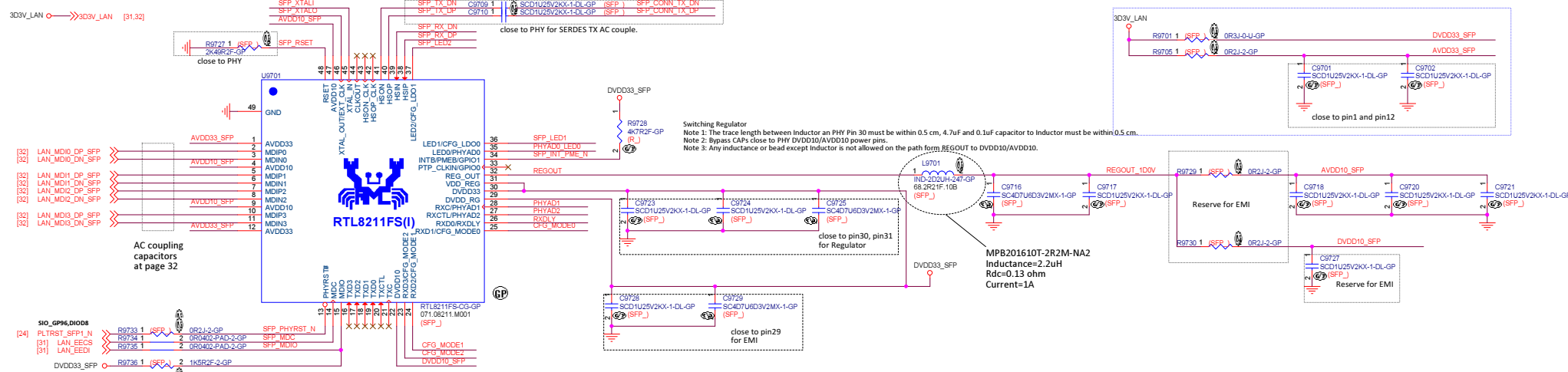
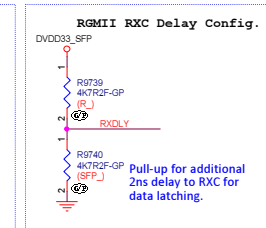
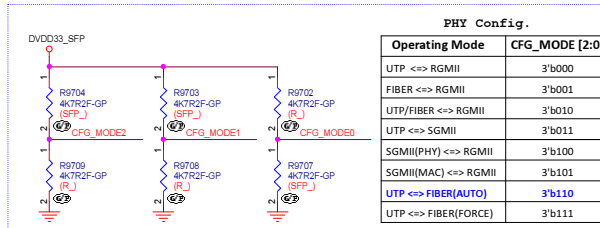
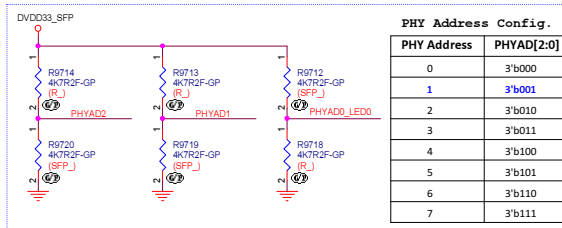
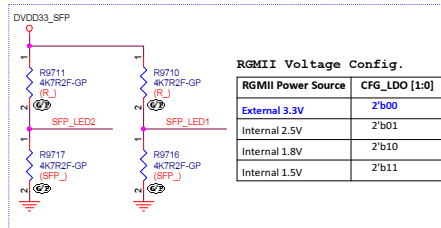
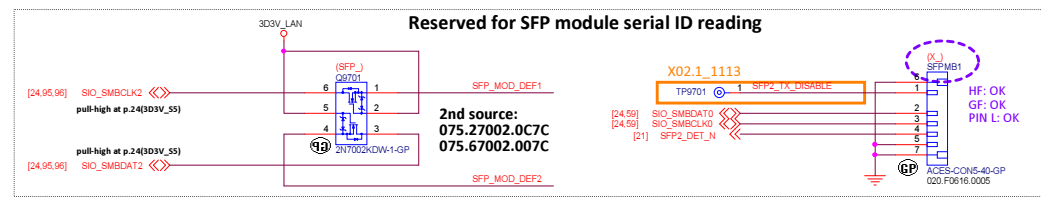
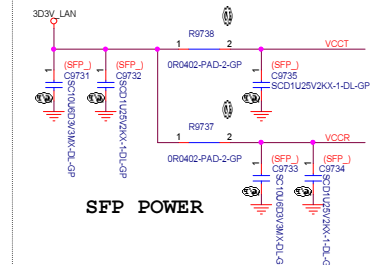
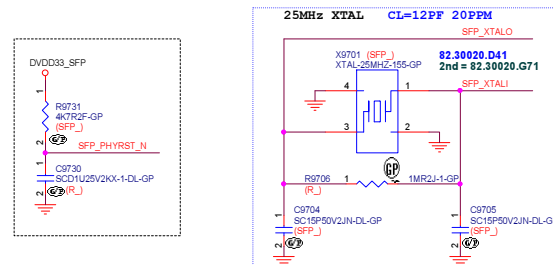
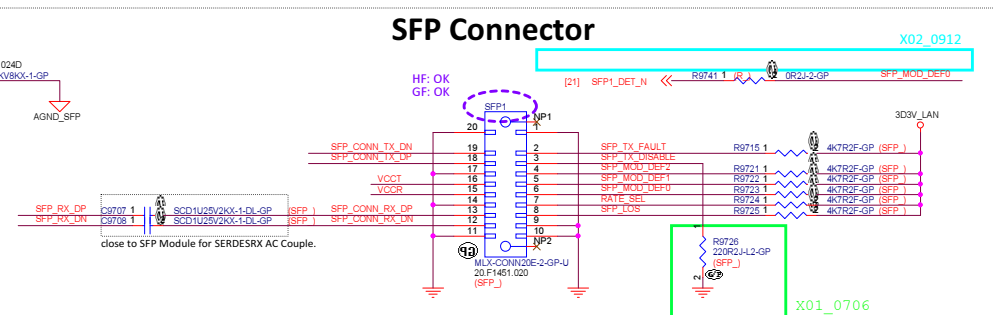
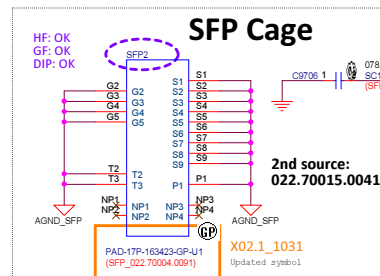


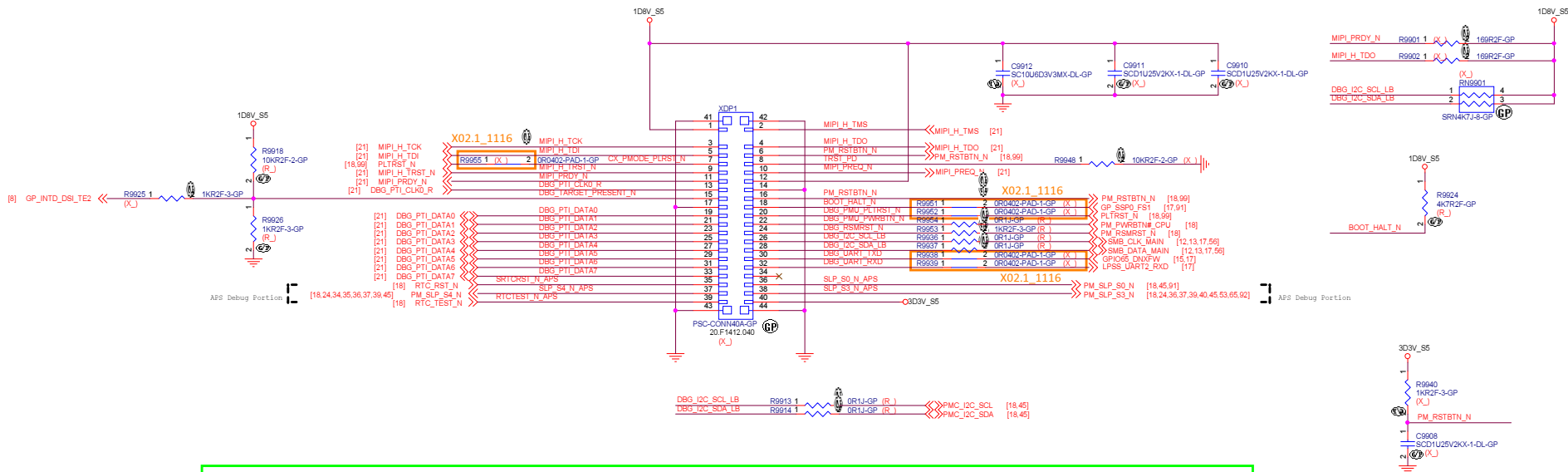
Figure 6. PHY Reset Timing (Internal Regulator)



Pitch: 0.8mm
Working voltage less than 36 volts (per pin)
Voltage: 50 Volts DC
Current: DC 0.7 Amperes AWG# 32

Blanking

1D8V_S5 1D8V_S5 [7,8,15,16,17,18,19,21,24,25,37,39,45,61,63,65,91]
3D3V_S5 3D3V_S5 [7,11,16,17,18,19,24,31,36,37,39,41,42,45,61,63,65,95,96]

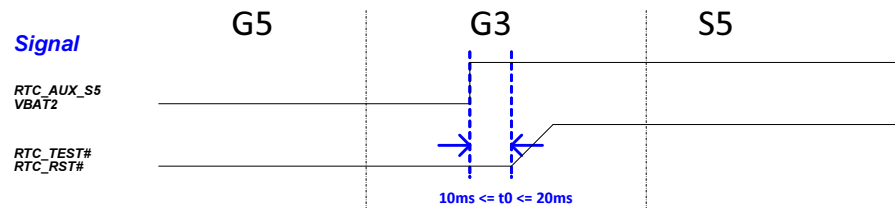


Blanking

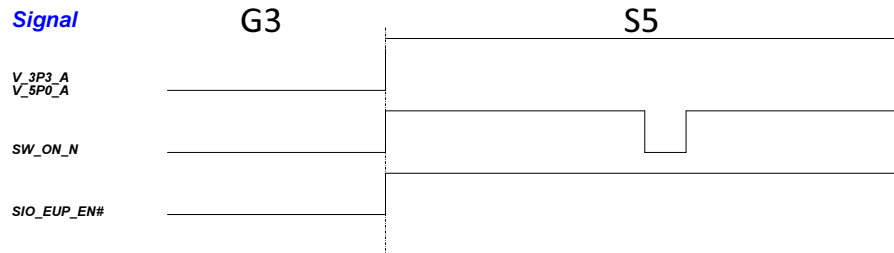
All cable part number for X02

Item	Cable List	Part Number	Description	Vendor	Dell PN	Dell Description
1	C.A. POWER SWITCH	350.06U01.0001	C.A. POWER_SWITCH_SANBERN_HT	Hgih-tek	MJD5F	ASSY,CBL,BTN,PWR,LED,5070
		350.06U01.0011	C.A. POWER_SWITCH_SANBERN_ICT	ICT		
		350.06U01.0021	C.A. POWER_SWITCH_SANBERN_VSO	VSO		
2	C.A. LEGACY BOARD	350.06U02.0001	C.A. LEGACY_1TO2_SANBERN_HT	Hgih-tek	JV09D	ASSY,CBL,PRL,PRT,5070EXT
		350.06U02.0011	C.A. LEGACY_1TO2_SANBERN_ICT	ICT		
		350.06U02.0021	C.A. LEGACY_1TO2_SANBERN_VSO	VSO		
3	C.A. SERIAL PORT	350.06U03.0001	C.A. SERIAL_PORT_SANBERN_HT	Hgih-tek	M32HC	ASSY,CBL,SER,PRT,2ND, 5070EXT
		350.06U03.0011	C.A. SERIAL_PORT_SANBERN_ICT	ICT		
		350.06U03.0021	C.A. SERIAL_PORT_SANBERN_VSO	VSO		
4	C.A. NET BOARD	350.06U04.0001	C.A. NET_OPTION_SANBERN_HT	Hgih-tek	P32XF	ASSY,CBL,NET,SFP,RJ45,5070
		350.06U04.0011	C.A. NET_OPTION_SANBERN_ICT	ICT		
		350.06U04.0021	C.A. NET_OPTION_SANBERN_VSO	VSO		
5	C.A. VGA BOARD	350.06U05.0001	C.A. VGA_OPTION_SANBERN_HT	Hgih-tek	CFX94	ASSY,CBL,VGA,5070
		350.06U05.0011	C.A. VGA_OPTION_SANBERN_ICT	ICT		
		350.06U05.0021	C.A. VGA_OPTION_SANBERN_VSO	VSO		
6	C.A. SERIAL BOARD	350.06U06.0001	C.A. SERIAL_OPTION_SANBERN_HT	Hgih-tek	MT0FM	ASSY,CBL,SERIAL,5070EXT
		350.06U06.0011	C.A. SERIAL_OPTION_SANBERN_ICT	ICT		
		350.06U06.0211	C.A. SERIAL_OPTION_SANBERN_VSO	VSO		
7	C.A. CAC BOARD	350.06U07.0001	C.A. CAC_CARD_SANBERN_HT	Hgih-tek	DG59X	ASSY,CBL,CAC, 5070,5070EXT
		350.06U07.0011	C.A. CAC_CARD_SANBERN_ICT	ICT		
		350.06U07.0021	C.A. CAC_CARD_SANBERN_VSO	VSO		

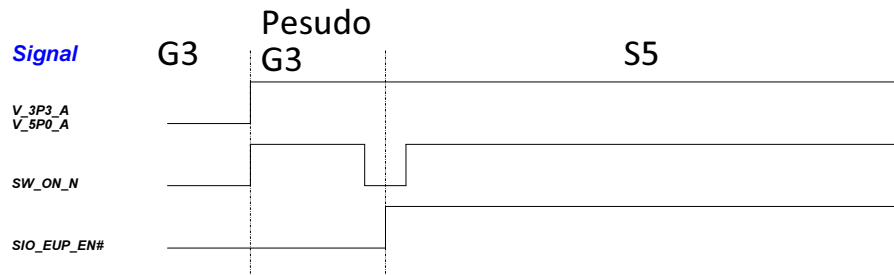
RTC Power Well Transition (G5 to S5 States Transition)



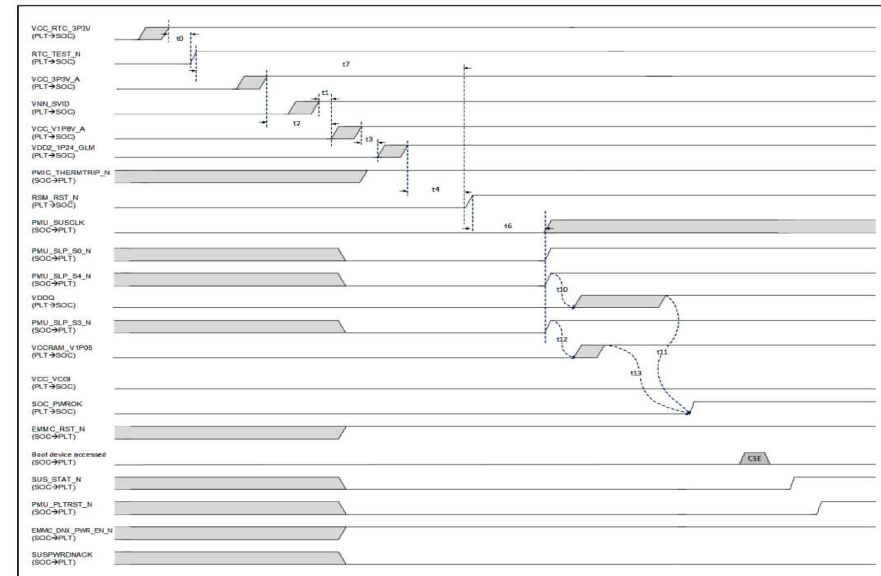
Power-up sequence(G3 to S5) ----- EUP Disable



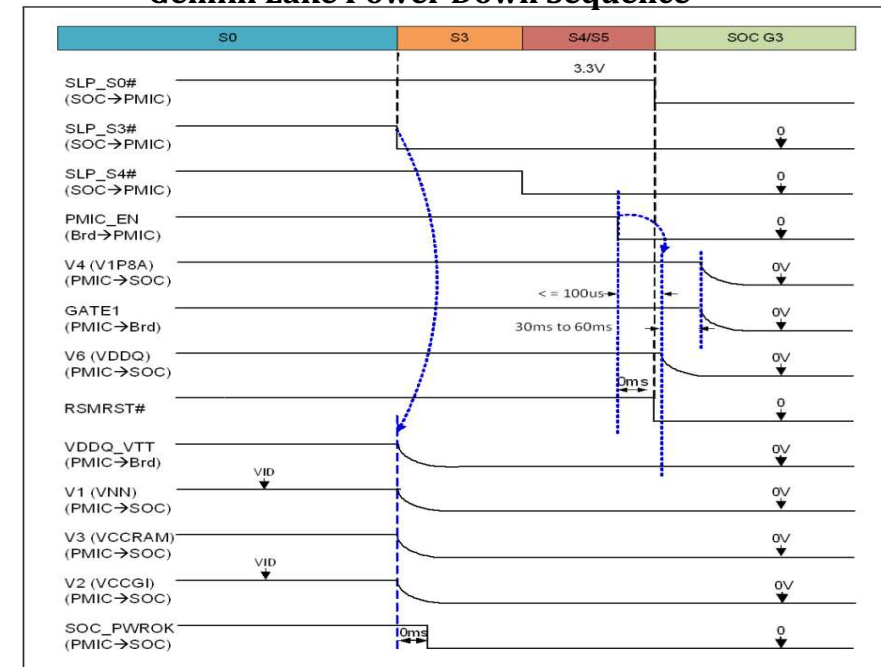
Power-up sequence(G3 to S5) ----- EUP Enable



Gemini Lake Power Up Sequence

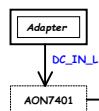


Gemini Lake Power Down Sequence

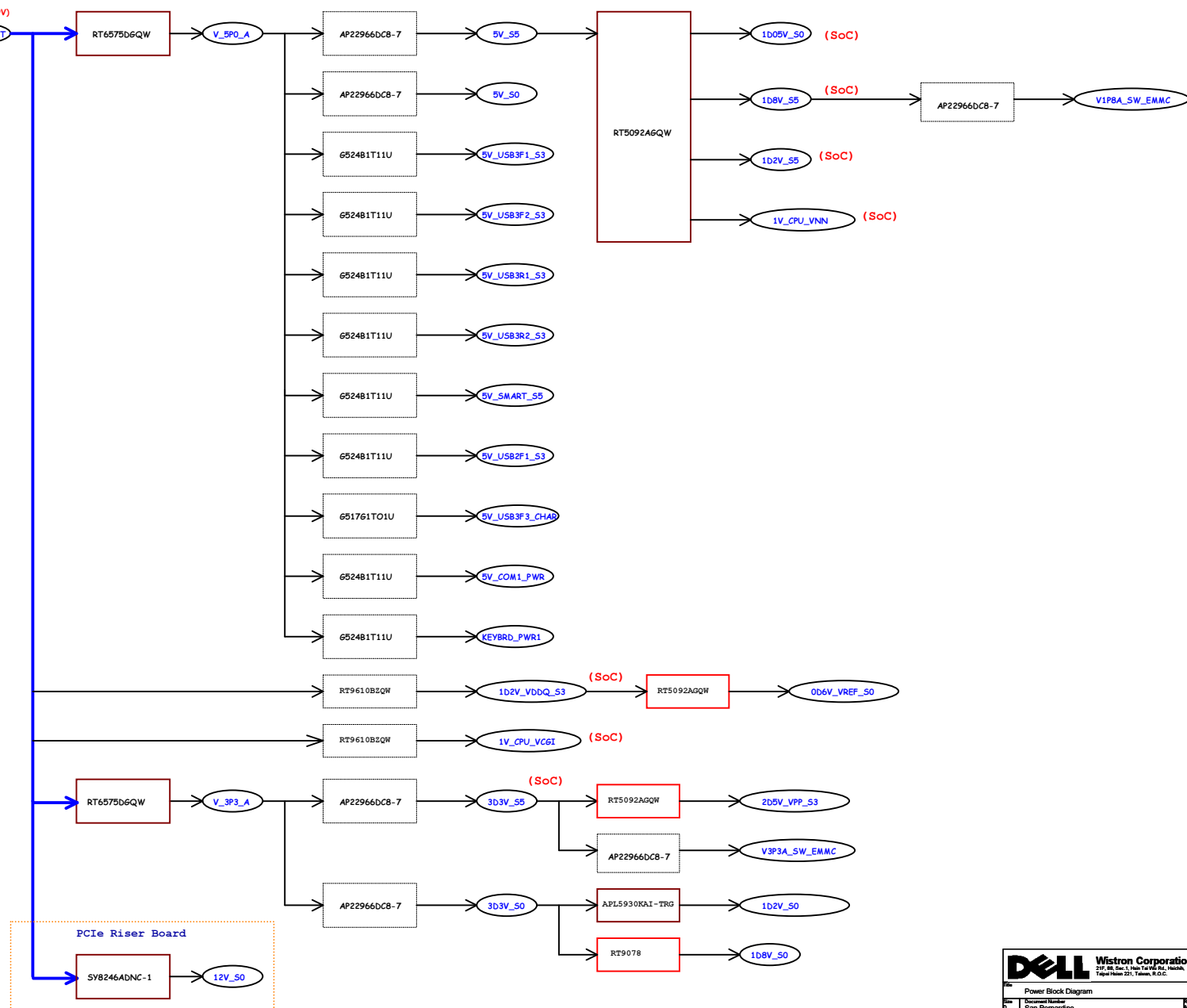
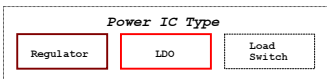


19V_DCBATOUT → 19V_DCBATOUT [62.84,45.45,45.85,9]
RTC_AUX_S5 → RTC_AUX_S5 [7.11,18.24,25,27]
V_3P3_A → V_3P3_A [34.25,40.41,44,54]
V_5P0_A → V_5P0_A [57.28,24.35,37.59,40.41,44,45,46,48,50,52]
3D3V_S5 → 3D3V_S5 [7.11,16.17,18.18,24.31,36.37,38.41,42,45,51,63,65,66,68,9]
5V_S5 → 5V_S5 [38.41,42,63,64,95,98]
3D3V_S5 → 3D3V_S5 [12.13,17.18,24,26,27,28,29,31,40,45,53,54,55,56,57,58,59,61,62,63,64,65,68]
5V_S5 → 5V_S5 [34.26,27,40,54,55,56,57,64,65,66,68,92,94]
1V_CPU_VNN → 1V_CPU_VNN [8,10,47,88]
1D8V_S5 → 1D8V_S5 [7.8,15,16,17,18,19,21,24,25,37,38,45,51,63,65,91,98]
1D8V_S5 → 1D8V_S5 [7,18,48]
2D5V_VPP_S5 → 2D5V_VPP_S5 [12,13,45]
1D2V_VDDQ_S5 → 1D2V_VDDQ_S5 [7,11,12,13,45,48,64,88]
0D6V_VREF_S5 → 0D6V_VREF_S5 [12,13,45]
1D8V_S5 → 1D8V_S5 [7,18,48]
1V_CPU_VCGI → 1V_CPU_VCGI [8,10,48,64]
1D8V_S5 → 1D8V_S5 [7,15,63,64,91]

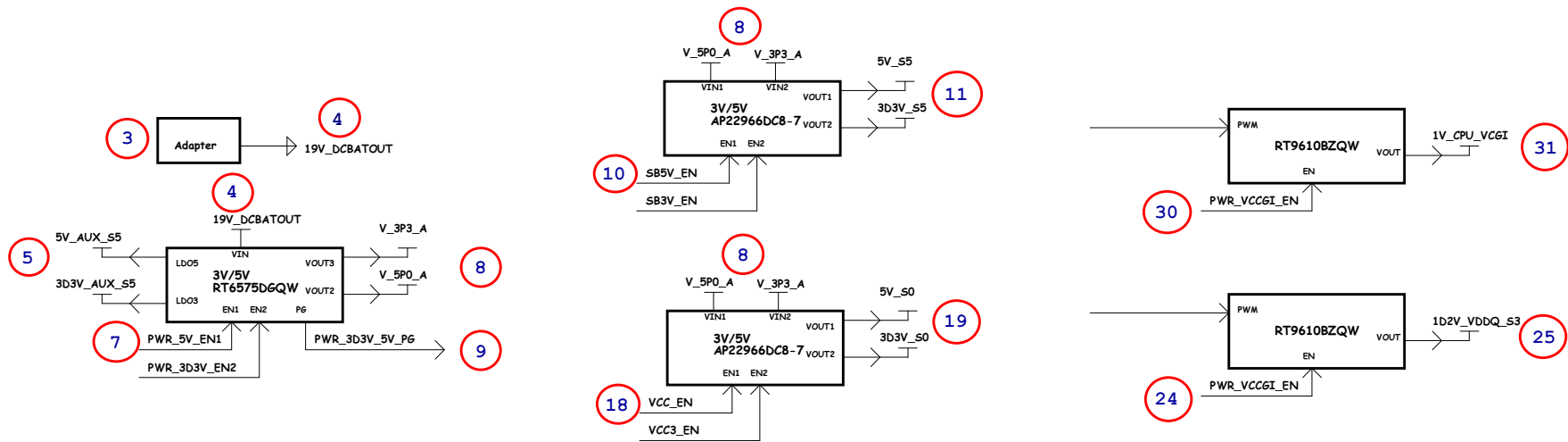
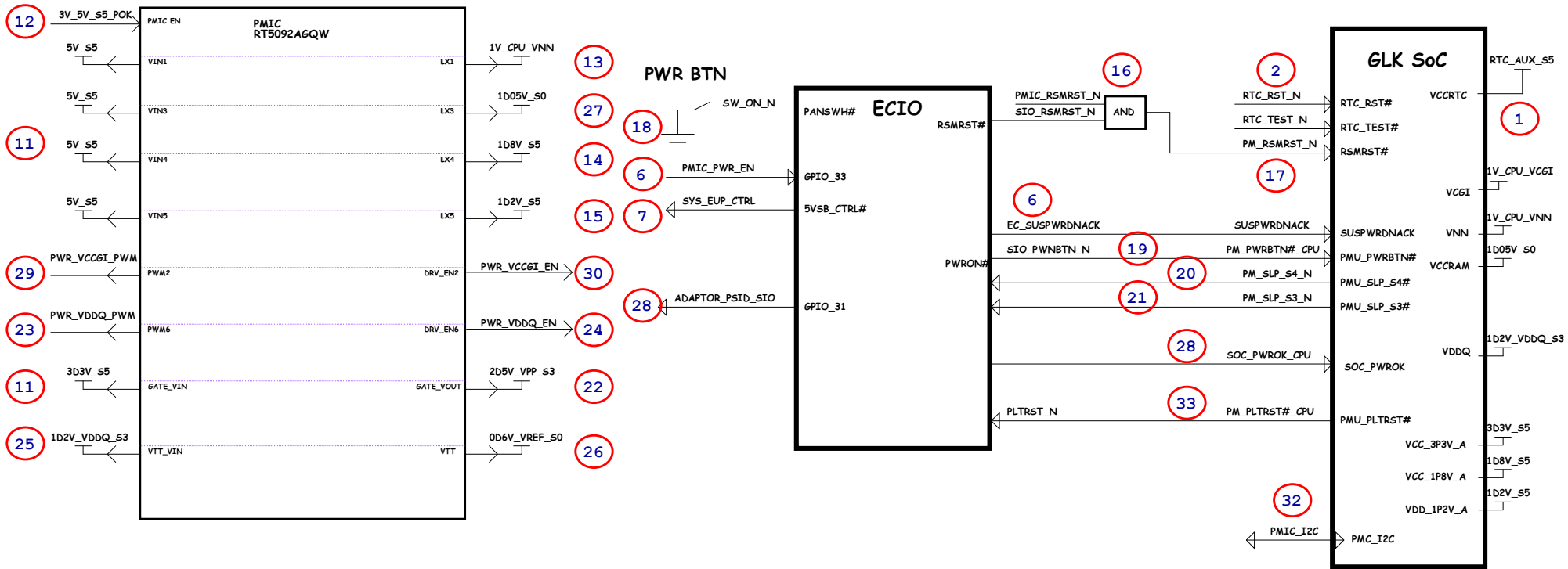
POWER: ADP-65W/90W/130W
OUTPUT: 19.5V

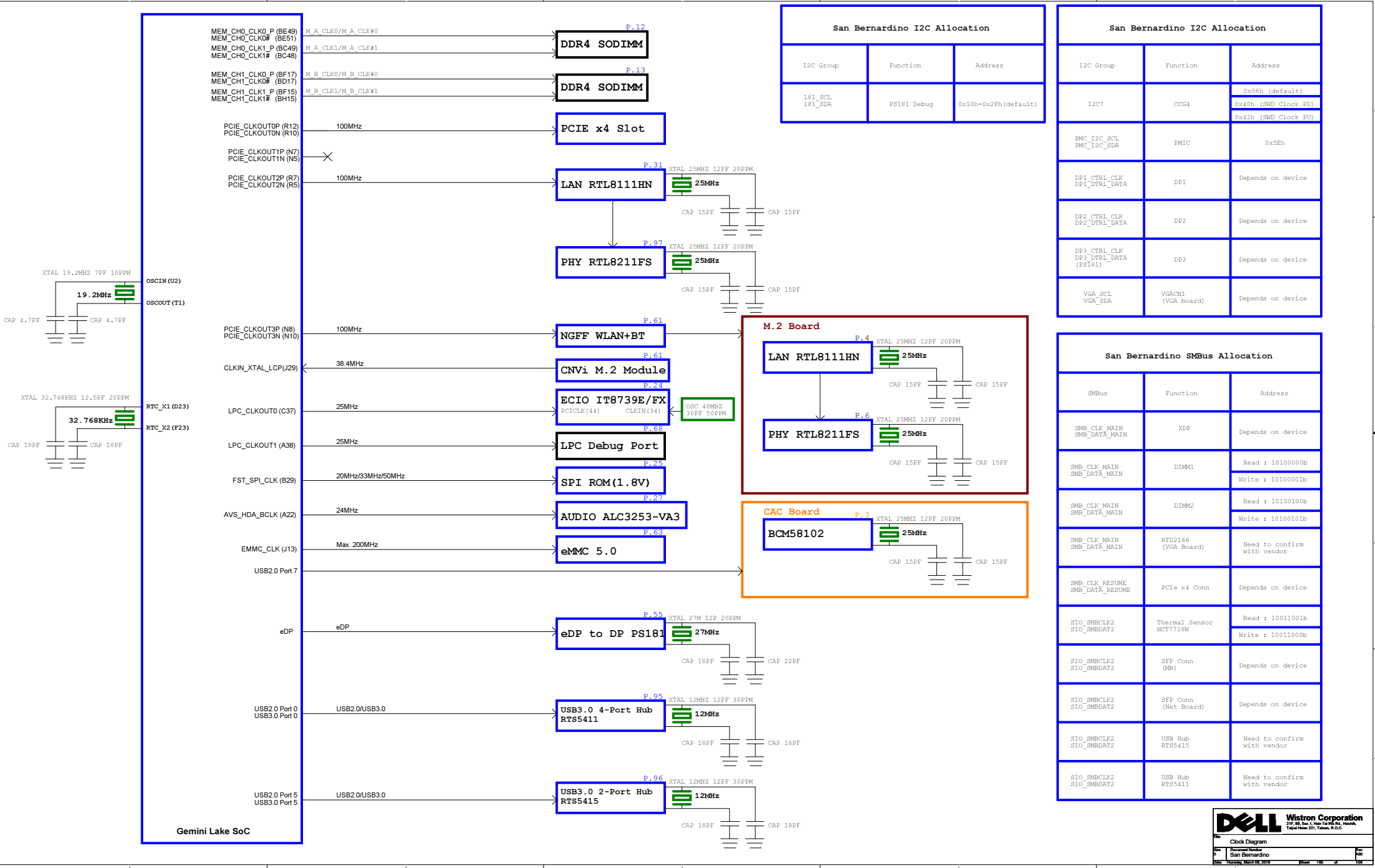


Wide Rang Input (19V)



GEMINI LAKE SEQUENCE & BLOCK DIAGRAM





San Bernardino I2C Allocation		
I2C Group	Function	Address
181_SCL 181_SDA	PS181 Debug	0x10h-0x2Fh (default)

San Bernardino I2C Allocation		
I2C Group	Function	Address
I2C7	COG4	0x08h (default)
		0x40h (SMD Clock PD)
		0x42h (SMD Clock PU)
PMC_I2C_SCL PMC_I2C_SDA	PMIC	0x5Eh
DP1_CTRL_CLK DP1_CTRL_DATA	DP1	Depends on device
DP2_CTRL_CLK DP2_CTRL_DATA	DP2	Depends on device
DP3_CTRL_CLK DP3_CTRL_DATA (PSI81)	DP3	Depends on device
VGA_SCL VGA_SDA	VGACN1 (VGA board)	Depends on device

San Bernardino SMBus Allocation		
SMBus	Function	Address
SMB_CLK_MAIN SMB_DATA_MAIN	XDP	Depends on device
SMB_CLK_MAIN SMB_DATA_MAIN	DIMM1	Read : 10100000b Write : 10100001b
SMB_CLK_MAIN SMB_DATA_MAIN	DIMM2	Read : 10100100b Write : 10100101b
SMB_CLK_MAIN SMB_DATA_MAIN	RTD2166 (VGA Board)	Need to confirm with vendor
SMB_CLK_RESUME SMB_DATA_RESUME	PCIe x4 Conn	Depends on device
SIO_SMBCLK2 SIO_SMBDAT2	Thermal Sensor NCT7718W	Read : 10011001b Write : 10011000b
SIO_SMBCLK2 SIO_SMBDAT2	SFP Conn (MB)	Depends on device
SIO_SMBCLK2 SIO_SMBDAT2	SFP Conn (Net Board)	Depends on device
SIO_SMBCLK2 SIO_SMBDAT2	USB Hub RTS5415	Need to confirm with vendor
SIO_SMBCLK2 SIO_SMBDAT2	USB Hub RTS5411	Need to confirm with vendor